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ACADEMIC PIPELINE AND FUTURES LAB

Brian D. Rigling

Wright State University

FEBRUARY 2016
Final Report

AIR FORCE RESEARCH LABORATORY
SENSORS DIRECTORATE
WRIGHT-PATTERSON AIR FORCE BASE, OH 45433-7320
AIR FORCE MATERIEL COMMAND
UNITED STATES AIR FORCE

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// Signature//

KELLY MILLER, Program Manager
Layered Sensing Performance Characterization Branch
Layered Sensing Exploitation Division

// Signature//

CHRISTINA SCHUTTE, Chief
Layered Sensing Performance Characterization Branch
Layered Sensing Exploitation Division

// Signature//

DOUG HAGER, Deputy
Layered Sensing Exploitation Division
Sensors Directorate

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14. ABSTRACT
The Cooperative Agreement under contract FA8650-09-2-1649 facilitated a host of collaborative projects between Wright State University and the Air Force Research Laboratory. As most of these projects were executed as independent efforts, our reporting reflects that structure. Each project is reported on separately in the pages that follow.

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sensors, automatic target recognition, carbon nano tube, radar, LADAR, software defined radio, surveillance

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1 SUMMARY

1.1 Abstract

“This funding will support the Academic Pipeline and Layered Sensing Futures Lab by developing synergistic hands-on projects for undergraduates during the summer as well as the academic year across several disciplines in the College of Engineering and Computer Science and College of Sciences and Mathematics at Wright State University.”

1.2 Results

The Cooperative Agreement under contract FA8650-09-2-1649 facilitated a host of collaborative projects between Wright State University and the Air Force Research Laboratory pursuit to the challenge presented in the abstract above. This final report presents an overview of the research and projects completed under this Cooperative Agreement, but the results are anything but final.

Literally hundreds of students have been impacted positively by the projects, mentors, networking, and exposure to research important to AFRL and our nation. These students, many now engaged as graduate researchers, are the real fruit of this vision and investment.

As most of these projects were executed as independent efforts, our reporting reflects that structure. Each project is reported separately in the pages that follow, and together add significantly to the body of knowledge required by AFRL’s mission. The period of performance of the Cooperative Agreement may be final and reports complete, but it’s continuing impact on the lives of the students and on the future of our nation is anything but final.

2 ATR CENTER SUMMER PROGRAM (prepared by F. Garber)

2.1 ATRC Summer Program 2011

The 2011 ATR Center (ATRC) summer program was housed in Building 620, WPAFB. The class of 2011 consisted of 10 summer interns and 6 visiting faculty guided by 14 AFRL mentors.

The summer program culminated with a Summer Workshop on "Performance-Driven Sensing, Performance Theory Challenge Problems" held at the Wright State University Nutter Center, 8-11 August, 2011. The summer workshop was held subsequent to the NATO Lecture Series on RADAR ATR and NCTR. Topics presented by ATR Center interns are shown in Table 1.

Table 1 2011 Summer Meeting Topics presented by ATR Center Interns.

3D Model Generation for Multi-Sensor Modeling Project	Ryan Blanford
Preprocessing for Electro-Optical Target Recognition	Shane Fernandes
LADAR Data Synthesis for Multi-Sensor Modeling Summer Project	Kristjan Greenewald
Argus Truthing Tool	John Hollkamp
Blender Animations	John Hollkamp
SAR Data Generation for Multi-Sensor Model Project	Tyler Keef
Government Algorithms for Tracking Exploitation Research	Andrew Kerns
CMA-HT, A Crowd Motion Analysis Framework Based on Heat-Transfer Analog Model	Yu Liang
A Sequential Framework for Image Change Detection	Andrew Lingg
Persistent Aerial Video Registration and Mosaicing	Edgardo Molina
Physics Accurate Layered Sensing Model	Rebecca Price
Feasibility of Joint Communication and Synthetic Aperture Radar (CoSAR)	Carl Rossler
A Probabilistic Relations Model	Chelsea Stiller
Moving Object Detection & Reconstruction for Audio-Visual Vehicle Classification	Tao Wang
Evolving Robust Gender Classification Features for CAESAR Data	Aaron Fouts
Persistent SAR Change Detection with Posterior Models	Gregory Newstadt
Geometric Prediction and Feature Extraction Of SAR Images	Chris Paulson
Polarimetric Infrared Exploration	Hamilton Clouse

We note that out of this remarkable Class of 2011, 4 intern alumni are now full-time employees in AFRL/RY.

The full-week agenda appears below. Individual intern briefings are available on the VDL here, with corresponding posters available here. Briefings and notes from the "Challenge Problem" sessions are available here.

NATO RTO & ATR Center Summer Workshop
AGENDA

Monday – NATO RTO Lecture Series

0830 Registration & Continental Breakfast
0900 Opening Ceremony & RTO Overview – National authorities
0915 Introduction – Prof. David Blacknell
0930 ATR of ground targets: Fundamentals – Prof. David Blacknell
1030 Morning Break
1100 ATR of air targets: Fundamentals & JEM – Mr. Peter Tait
1120 Lunch Break
1330 Single / full polarization ATR – Dr. Les Novak
1430 Multi-Aspect ATR – Prof. Hugh Griffiths
1530 Afternoon Break
1600 Comparing Classifier Effectiveness – Dr. Joachim Schiller

Tuesday – NATO RTO Lecture Series

0900 Databases & Modelling – Prof. David Blacknell
1000 Morning Break
1030 Air targets: Helicopters & Range-Doppler – Mr. Peter Tait
1130 Knowledge-based techniques – Prof. Hugh Griffiths
1230 Lunch Break
1400 SAR Change Detection – Dr. Les Novak
1500 Afternoon Break
1530 Round Table Discussion
1730 Dinner

Wednesday – ATR Center and Center for Surveillance Research Student Day

0830 Registration & Continental Breakfast
0900 Welcome and ATR Center Overview – E. Zelnio, AFRL/RYA
0915 CSR Overview – B. Rigling, WSU
0930 ATR Center presentations – ATR Center students
1100 Lunch Break
1330 CSR presentations – CSR students
1500 Poster session – ATR Center and CSR students
1800 CSR Review and Board of Directors meeting.

Thursday – Future Research Directions: Challenge Problem Definitions

0830 Continental Breakfast
0900 Challenge Problem: Detection – R. Willett, Duke
0930 Discussion & Refinement
1000 Challenge Problem: Tracking – SIG or COMPASE
1030 Discussion & Refinement
1100 Lunch Break
1300 Challenge Problem: Recognition – BUMP
1330 Discussion & Refinement
1400 Challenge Problem: Reconstruction – R. Moses, OSU
1430 Discussion & Refinement
1500 Challenge Problem Space Synthesizing and Prioritizing
1600 Challenge Problem Restatement and Recap

2.2 ATRC Summer Program 2012

The 2012 ATR Center summer program was housed in Building 620, WPAFB. The class of 2012 consisted of 40 summer interns and 2 visiting faculty guided by 20 AFRL mentors. Total costs attributed to the summer program were approximately $561,000.

The summer program culminated with a Summer Meeting on “Performance-Driven Sensing, Performance Theory Challenge Problems” held at the Wright State University Nutter Center, 15-16 August, 2012. The summer workshop was held subsequent to the Center for Surveillance Research Review. An overview of the Summer Meeting Topics presented by ATR Center interns is shown in Table 2.

Table 2 2012 Summer Meeting Topics presented by ATR Center Interns.

Patrick Doran	Video Georegistration Truthing
David Nicodemus	Integrated Simulation Environment to Test Different Georegistration Approaches
P. Evan Linn	An Analysis of RF Scattering Statistics
Phillip Atkins	Target Decompositino for Efficient Signatures Production
Rebecca Boyer	Multi-Sensor Modeling Project 2: Particle Effects
Ryan McCoppin	Effects of Clothing on Gender Classification
Jacob Ross/Greg Bryant	Data Archive and Tretrieval Examination (DARE) Project
Andrew Johnson	GATER GUI Development
Taylor Edmiston	GATER Comms: A Real-time Module Communications Library and Architecture
Xueyu Hu	Improving Algorithm Speed with Matlab
Shane Fernandes	Vehicle Observation and Isolation by Chipping Extracted Data (VOICED)
Aileen Duckett	Automatic Target Recognition (ATR) of Vehicles in Electro-Optical (EO) Imagery Using Template Matching Algorithms
Kevin Saich	Signatures and Phenomenology Measurement Test Bench (SPMTB)
Ryan Blanford	3D Model Generation for Multi-Sensor Modeling Project
Kristjan Greenewald	LADAR ATR Performance Prediction
Rebecca Price	Electro-Optical Synthetic Civilian Data Domes
Dr. Liang	Vehicle Tracking and Analysis in a City
Gabrielle Vanderburgh	ATRpedia Organization Project
Sean O'Rourke	Adaptive Field-of-View Tracking and Association for Multimodal Sensors
Matthew Spradlin	Large Scale Physics Accurate Layered Sensing Model
Frank Golub	Signature Phenomenology Analysis Bench
Jeremy Vila	Hyperspectral Image Unmixing via Bilinear Approximate Message Passing
Matthew Bischoff	Computational Electromagnetics in ATR
Rebekah Farrar	Step-Length Estimation Using Radar
Scott Altrichter	Polarimetric SAR Imaging of Extended Targets from Real Data
Michael Levy	Cramer-Rao Type Bounds for Biased Estimators
Michael Riedl	Combining Synthetic Aperture Radar and Space-Time Adaptive Processing using a Single-Receive Channel
Carl Rossler	Feasibility of Join Communication and Synthetic Aperture Radar (CoSAR)
Andrew Lingg	Cramer-Rao Lower Bound on Feature-Based Projective Image Registration
Christopher Paulson	Classificaiton of Civilian Vehicles Using Glint Phenomenology
Greg Newstadt	A Generalizable Hierarchical Bayesian Model for Persistent SAR Change Detection and Tracking
Linda Bai	Compressive radar clutter estimation with dictionary learning
Aaron Myers	AFIT Random Noise Radar Applications
Josh Ash	Incorporating Spatial Structure into Bayesian Hyperspectral Scene Analysis
Capt Hammond	Canonical Feature Extraction using Molecule Dictionaries, Matching Pursuit, and Bayesian Estimation
Capt M. David Archer	Effectiveness of MGL-S8A B-dot Sensor in Airborne High Frequency Magnetic Field Direction Finding
Maj Jeremy Stringer	Wideband Adaptive Beamforming for Application to an ES Receiver
Mike Temple	RF-DNA Fingerprinting "Distinct Native Attributes"

The Workshop agenda appears below. An ATRpedia page with comprehensive active- links to: intern personal pages, intern project pages, intern briefings, intern posters, and AFRL mentor pages (see snapshot in Table 3 below) is available on the VDL here.

Table 3 Sample of 2012 Workshop Agenda Page.

ATR Center Projects *Summer 2012* [edit]

ATR Center 10-minute Briefings [hide]

Name	Talk	Briefing	Poster	Affiliation	Rank	Mentor(s)/Colleague(s)	Branch
Frank Golub	Signature Phenomenology Analysis Bench ***See also:*** *Signatures and Phenomenology Measurement Test Bench (SPMTB)*	GolubFrank2012	GolubF2012	Ohio State University	Graduate Student	Dr. John Malas Dr. Mike Saville	RYAS
Rebecca Boyer	Multi-Sensor Modeling Project 2: Particle Effects	BoyeR2012	BoyeR2012	Wright State University	Undergraduate Student	Todd Rovito	RYAT
Greg Newstadt	A Generalizable Hierarchical Bayesian Model for Persistent SAR Change Detection and Tracking	NewsG2012	NewsG2012	University of Michigan	Doctoral Student		
Matthew Bischoff	Computational Electromagnetics in ATR	BiscM2012	BiscM2012	Wright State University	Graduate Student (Physics)	Dr. Mike Saville	RYAS
Ryan McCoppin	Effects of Clothing on Gender Classification	McCoR2012	McCoppinR2012	Wright State University		MENTOR	RYAT
Christopher Paulson	Classification of Civilian Vehicles Using Glint Phenomenology	PaulC2012	PaulC2012	University of Florida	PhD Candidate	Ed Zelnio	RYAT
Andrew Johnson	GATER GUI Development	JohnsonA2012	JohnsonA2012			MENTOR	RYAT
Taylor Edmiston	GATER Comms: A Real-time Module Communications Library and Architecture	EdmiT2012	EdmiT2012	Wright State University	Graduate Student	MENTOR	RYAT

Wednesday, 15-August – ATR Center and Center for Surveillance Research Review

0800 Registration & Continental Breakfast
0830 Welcome and ATR Center Overview – E. Zelnio, AFRL/RYA
0840 ATR Center and CSR Presentations (10 Min each)
1030 Break
0840 ATR Center and CSR Presentations (10 Min each)
1200 Lunch *in situ*
1230 ATR Center and CSR Presentations (10 Min each)
1500 heavy hors d'œuvres
1500 Poster session – ATR Center and CSR students

Thursday, 16-August – ATRC & CSR Directions, Challenges, Programs

0800 Continental Breakfast
0830 Technical Directions – Government Perspectives
1000 Break
1030 Technical Directions – University Perspectives
1200 Lunch
1300 Challenge Problem: Reconstruction, 3D - OSU
1315 Challenge Problem: Reconstruction, 2D - WSU
1330 Challenge Problem: Recognition, SAR – OSU
1345 Challenge Problem: Recognition, LADAR - Jacobs
1400 Break
1430 Panel Discussion
1530 Programmatic Directions

2.3 ATRC Summer Program 2013

For the first time, the 2013 ATR Center summer program was housed at Wright State University in the Russ Engineering/Joshi Center Complex. The class of 2013 consisted of 48 summer interns and 3 visiting faculty guided by 25 AFRL mentors. Total costs attributed to the summer program were approximately $925,000.

The summer program culminated with a Summer Review focusing on "Performance-Driven Sensing, Performance Theory Challenge Problems" held at the Wright State University Nutter Center, 12-16 August 2013. The ATR Center summer review was held circumjacent with The Center for Surveillance Research Review and a review of the DARPA KeCom program with the agenda appearing below.

KeCom/CSR & ATR Center Summer Review

AGENDA

Monday, 12-August – Principles and Practice of Bayesian Inference

1230 Bayes 101 – Greg Newstadt
1310 Sampling Techniques – Greg Newstadt
1410 Break & Homework
1430 Applications: SAR, GOTCHA – Greg Newstadt
1500 Belief Propagation Primer – Josh Ash
1545 Break & Homework
1630 Applications: Hyperspectral Sensor Exploitation – Josh Ash

Tuesday, 13-August – KeCom Review Sampler

0900 Compressive Sensing Primer – Phil Schniter
0945 AMP Tools for Large Scale Inference – Phil Schniter
1045 Break/Discussion
1100 Adaptive Sensing – Phil Schniter
1130 Design of Active Measurements for Compressive Classification – Emre Ertin
1245 Lunch
1400 Change Detection – Josh Ash
1430 Break
1500 Duke Team Topics – Patrick Lull

Wednesday, 14-August – Center for Surveillance Research Program Review

(CSR members and AFRL Govt. personnel)

Thursday, 15-August – ATR Center Summer Intern Review

0800 Continental Breakfast
0820 Welcome and ATR Center Overview – E. Zelnio, AFRL/RYA
0830 ATR Center and CSR Presentations (10 Min Max)
1000 Break
1020 ATR Center and CSR Presentations (10 Min Max)
1200 Lunch
1300 ATR Center and CSR Presentations (10 Min Max)
1500 Heavy hors d'œuvres AND
1500 Poster session – ATR Center, CSR, AFIT, etc.

Friday, 16-August – Mentor and Planning Day (ATR Center Principals)

0800 Continental Breakfast
0830 Mentor presentations
1030 Break
1030 Challenge Problems: LADAR, SAR, Reconstruction
1200 Lunch
1300 Sensor Measurement Tools
1500 Break
1520 Future Methods & Metrics

An ATRpedia page with comprehensive active-links to: Summer review briefings on Bayesian inference, review briefings for the DARPA Knowledge Enhanced Compressive Measurement (KECoM) program, and links to intern briefings and posters, along with mentor planning, is available on the VDL here with a page preview shown below.

Name	**Mentor**	**Title** (links to poster)
Christopher Menart	Ed Zelnio	Scattering Operators for Invariant Feature Representation
Evan Linn	Mike Callahan	Estimating Clutter Rank
Frank Golub	Ed Zelnio	Joint Imaging and Scatterer Anisotropy Estimation
Kristjan Greenewald	Ed Zelnio	Detection of Anomalous Crowd Behavior Using Spatio-Temporal Kronecker Sum Decompositions
Dalvir Saini	Mike Saville	Classifying Civilian Vehicle with Wide-Angle Polarimetric SAR using Attributed Scattering Center Model
Nate Monnig	Sam Sakla	Sparse Representation for Vehicle Recognition
Benjamin Sommerkorn	Mike Saville	Bistatic Manifold and Resolution Determination
Mark Connor ~ Best Briefing	John Malas	Signature Phenomenology Measurement Test Bench
Austin Mackey	Brian Rigling	Raider Tracer Bistatic
Erik Schembor	Mike Saville	Efficient Simulation of Bistatic SAR
Shih-Ling Phuong	Mike Saville	Investigation of PO Integral for Bistatic Scattering Project
Jason Brand	Jeffrey Allen	Electromagnetic Source Transformations
Ryan Blanford	Linda Moore	Wide Angle SAR Imaging Project
Alexander Gutierrez	Jason Parker	Interferometric Inversion in Radar Imaging
Michael Riedl	Michael Minardi	Joint Synthetic Aperture Radar and Space Time Adaptive Processing on a Single Receive Channel
Jeremy Vila	Jason Parker	An Empirical-Bayes Approach to Recovering Linearly Constrained Non-Negative Sparse Signals
Brigid Blakeslee ~ Best Briefing	Ed Zelnio	Simultaneous Inference and Control for Improved Object Identification
Sean O'Rourke	Muralidhar Rangaswamy	Adaptive Field-of-View Multitarget Tracking for Multimodal Sensors
Eliza Straughter	Jim Leonard	Is There Any Information Hidden in the Sky?
Aileen Duckett	Richard Van Hook	Minor Area Motion Imagery (MAMI)
Nathan Rude	Mateen Rizki	Electro-Optical Seasonal Weather and Gender Data Collection
Ryan McCoppin	Mateen Rizki	SWAG Gender Classification Experiment and Analysis
Rebecca Price	Todd Rovito	Projection Tool Box
Andrew Profeta	Andres Rodriguez	Configuring Neural Networks
Ishan Paranjpe	Clark Taylor	Vision Aided Navigation
Bevin Duckett	Olga Mendoza-Schrock	Truthing with SICK Lasers
Lauren Crider ~ Best Poster	Scott Kangas	Exploiting Vibration-Based Signatures for Automatic Target Recognition
Spradlin, Henderson, Greenewald	Todd Rovito, Darrell Barker, Ed Zelnio	Fiorano: Detection Test Bed - Modeling
Sanderson, Wittman	Todd Rovito, Darrell Barker, Ed Zelnio	Fiorano: Detection Test Bed - Truth and Performance Modeling
Gabrielle Vanderburgh	Ed Zelnio	ATRpedia Design Project
Taylor Edmiston	Juan Vasquez	Low-resolution Augmented Track Elimination Routine (LATER)
Andrew Johnson	Juan Vasquez	Fragment Association Matching Enhancement (FAME)
M. Rangaswamy	N/A	Rank Constrained Covariance Matrix Estimation & Application to Radar STAP
Sajal Kantha	James Patrick	WAMI Automated Truth Evaluation
Shane Fernandez, Stephen Sweetnich	Wesam Sakla, Jeffrey Clark	Hyperspectral Fusion Exploitation for Management of Multiple-Sensor Assets (HFEMMA)
Mike Menart, Kevin Conley	Clark Taylor	Onboard Processing for Surveillance UAVs

3 WSU ACADEMIC PIPELINE AND LAYERED SENSING FUTURES LAB (prepared by K. Xue)

3.1 Integration with Other Programs

The work will synergistically link several ongoing and planned research and educational programs from several organizations to create a sustainable, year-round, experiential learning program that will provide students with skills and experiences to move them along the Academic Pipeline (high school, undergraduate, graduate, and post-doctorial) and prepare and inspire them for the high-tech workforce within academia, the DoD and industry. This will be done in an educational context by utilizing cutting-edge technology being developed to attack real-world problems. Tec^Edge will play a central role in the integration of students under this highly collaborative program.

3.2 Accomplishments during Period of the Agreement

- The WSU faculty, staff, and students worked with several other organizations and programs in the Dayton Area and external to the Dayton area. These included:
    - The significantly leveraged partnership between AFRL, the Wright Brothers Institute, WSU, AFIT and several other organizations and companies via collaborative environment and resources at Tec^Edge and the Discovery Lab. Project collaborations included Mound Laser and Photonics Center, Miami Valley Career Technology Center, Qbase, WSU College of Nursing, Miami Valley Hospital / Premier Health Partners, TecEdge Works, Designing Digitally, and others.
    - Shared activities with the AFRL Summer Internship program for undergraduate and high school students, such as the AFRL summer interns program, Wright STEP and Wright Scholar programs.
        - Virtual Discovery Lab (ViDL) is an important focus area that has been expanded to maintain student collaborations throughout the years and at multiple locations simultaneously.
- Number of Participants over the period of the Agreement: SATE program started in 2008 with over forty (40) undergraduate students. The YATE program established in 2011 which is a relatively smaller scale around year undergraduate research learning program. YATE program aimed to develop student project leaders for the SATE programs. The following table listed the number of student participants over the years.

Table 4 Student Participation by Year/Program, 2008-2011.

Year	SATE	YATE (Fall quarter 2011)	YATE (Winter quarter 2012)	YATE (Spring quarter 2012)
2008	>40			
2009	>60			
2010	104*			
2011	>110	43	20	28

*Including 14 high school students.

In the Fall of 2012, Wright State University converted from a quarter academic calendar to a semester academic calendar.

Table 5 Student Participation by Year/Program, 2012-2015.

Year	SATE	YATE Spring	YATE Fall
2012	125		55
2013	89	55	37
2014	70	33	3
2015	7		

- Students that participated the research learning programs were from a wide variety of institutions:
    - High Schools: Temple City High School, Centerville High School, Beavercreek High School, Middletown High School, Dayton Christian High School, Springboro High School, Lakota West High School, New Albany High School, MVCTC, South Carolina Governor's School for Science and Mathematics, etc.
    - Colleges and Universities: Columbus State Community College, Sinclair Community College, Cincinnati State Technical and Community College, TCC, University of Louiville, University of Missouri, Harding University, Denison University, Case Western Reserve University, University of Cincinnati, Cornell University, Ohio University, Georgia Institute of Technology, Western Carolina University, Worchester Polytechnic Institute, Massachusetts Institute of Technology, Carnegie Mellon University, University of Dayton, University of Maryland, The Ohio State University, University of Wisconsin at Eau Claire, University of Toledo, University of Akron, University of Findlay, University of Michigan, University of Arizona, Miami University (Ohio), Wright State University, etc.

3.3 Recruitment

Recruitment of students will include efforts at Dayton area universities and community colleges for the academic year program and at the local and national level for summer time programs. The Academic Pipeline will also work with other programs at AFRL and with other universities and organizations to ensure the broadest and most effective impact.

- Continuous recruitment has been maintained for the Wright^Edge Academic Pipeline Scholarship via a webpage and networking. Materials provide an overall description of the scholarship program, contract information, and an application that can be submitted on-line. (For example see: https://www.engineering.wright.edu/ee/wright-edge-scholarship.phtml).
- Faculty and student networking at Discovery Lab (Tec^Edge), WSU and other Dayton area organizations were also utilized, particularly for YATE. SATE recruitment also utilizes other AFRL summer internship programs.
- Recruitment reached to students not only in the south-west of Ohio region but also in the national level.

3.4 Academic Components

Through project mentorship by university faculty, government and industry scientists and engineers and through workshops and seminars, students will become better prepared for the next level of the Academic Pipeline and understand the important role that research plays in the development of new technologies. Students will be made aware and prepared for additional educational opportunities, such as graduate school in a STEM field.

- Each specific research learning project has several common core components related to the student's education. These include a mentor for relevant experiential research project with specific goals, a team of students, technical milestones to achieve during the duration of the projects, communication milestones, and the project leave behinds. This is modeled after engineering Senior Projects that are 10-20 weeks in length. This model includes a significant problem to be solved by a team/group effort. While the technical tasks vary with each project, each group will prepare a poster, final technical report, movie of the project, and pre-pare leave-behinds so the project can continue with the next student group.
- In each research experiential learning project, students are going through the process of project idea proposal, design, design review, implementation, testing, and presentation of project results in a publicly held SATE conference.

3.5 Projects

Experiential, student-centered projects are the cornerstone of the APL. Students will be paired with university faculty, government and industry scientists and engineers that will provide educational and project mentorship for the students. These projects will vary in size, length and scope and will be linked to on-going technology interests to provide a high level of motivational and educational relevance to the students.

- A partial list of student-centered research experiential learning projects:
    - 3D Music Box: Using skeletal tracking technology and generative model to create music
    - AVATAR (Advanced Virtualization for Adversary Tracking and Anticipatory Response): seamless integration of real and virtual worlds so that virtual worlds can be utilized to predict and manage real world events.
    - CAMPA (Cued Anamnesis Model Password Algorithm): developed a method for creating super-strong passwords that will be remembered quicklyand easily.
    - CASSI (Capacity Assessment Software System Implementation): combine the principles of artificial intelligence and data mining that demonstrates proof-of-concept capability for assessing the capacity of manufacturing machines, planning, and analysis in production facilities in real time.
    - Cyber Sentinel: Maintain a level of security for the virtual environment. This was accomplished by being able to detect users entering the virtual world and track the avatar's GPS locations in real time.

- Digital AVATAR Presence Robot: Focuses on utilizing an Android tablet to control the movements of a turtlebot in the physical world while simultaneously moving a virtual robot in the virtual world.
- Direct Metal Laser Sintering: Additive Manufacturing technique that uses a high powered laser and metal powder in order to form a 3D part.
- Dragonfire: Design a flying quadrotor unconstrained by the typical battery life with the capability to receive information from the surroundings.
- Eagle Eye: utilizes social media and augmented reality to help reduce the response time of emergency relief units.
- GeoSeek A game designed to teach Geospatial Intelligence principles to fifth graders.
- GridToGo: Fill the currently empty niche of a simple, self-contained program to create and manage decentralized OpenSim grids.
- Guardian Angel: UAV sensing Android App
- Holodeck: Create an immersive virtual environment using the Emotiv headset and the Microsoft Kinect.
- Humanoid Robotics with NAO: Project set out to combine complex methods of computer vision and control in a humanoid robot to create behaviors never before demonstrated on the NAO robot from Aldebaran Robotics.
- O-B-1 Utilizing the Microsoft Kinect to gather 3D point cloud data that can be seen in Virtual World so that we may better display real world environments or people and give the feeling of being "physically there."
- Operation P.A.N.I.C.: The application enables the user to record video, audio, and capture images and send them to a server.
- Pocket-VDC: Create a framework to access the OpenSim virtual environment using an Android device
- Save-the-Soldier: Partnered with Wright State's School of Medicine (Surgery Surgical Simulations department) to investigate virtual reality, and app development to train medical residents on how to properly treat lower extremity wounds.
- Swiss Army Knife Bot: Create a multi-purpose, modular robot capable of multiple types of ground and air movement.
- Robotic Telepresence and Team Telerobotics: Implement robotic telepresence using a tablet and a commercially available robotic platform.
- TLQRMAV: Tube Launched Quadrotor and Fixed Wing Micro Air Vehicle
- Virtual Geoint Center: Command center is designed to be a virtual platform for incoming

3.6 WSU Layered Sensing Futures Lab

WSU will establish a Layered Sensing Futures Lab to support the Academic Pipeline by making projects available for continued development through course work, senior design projects, and other academic STEMM related activities at WSU and in the greater Dayton region. This dedicated laboratory space will serve as a central location for sensor algorithm and hardware development and will be considered student project space and a user facility for those in the supporting the Academic Pipeline.

3.6.1 Accomplishments during Reporting Period

- The WSU Layered Sensing Futures Laboratory (WrightEdge) facility (room 142 and subsequently room 233 in Russ Engineering Center) were utilized for project activities by the YATE and Summer SATE students with 24/7 access.

3.7 Collaborative Opportunities for Research Experiences (CORE) Team

A CORE team will be established that will consist of faculty from several departments and colleges at WSU as well as a group of graduate and undergraduate students linked to the faculty and the other programs the Academic Pipeline synergistically works with, such as Tec^Edge and IDCAST. This CORE team will be the link between AFRL and industry and the vast set of academic and research resources at WSU and will work to provide mentorship and develop new project topics for students in the Academic Pipeline.

- Continued involvement by WSU from: Dres. Kefu Xue, Dr. Petkie and Mr. Bob Myers (Wright State Research Institute) with support from Mrs. Vickie Slone and Mr. Tony Tritschler from the Electrical Engineering Department.
- Continued partnership with the Discover Lab (Tec^Edge) Director, Dr. Robert Williams, and Tec^Edge scientists and engineers.

3.8 Student and Program Assessment

Wright State will develop an assessment program that will provide feedback on the impact the program has on students and the student's perception of their project, development of their skill set, the impact on their career choices and perception of the academic, government and industry partners they worked with.

- Informal feedback with written document/video/other media is provided by the students to the mentors.

4 WAVEFORM DESIGN FOR STAP (prepared by P. Setlur)

Research for waveform design for radar space time adaptive processing (STAP) and waveform design for radar using information theory. Our results were published in the IEEE Radar Conf. 2013, Ottawa, CA and in the IEEE Radar Conf., Cincinnati, OH. Our main contributions can be seen in the papers presented at these conferences and is available on IEEE explore. Below we present the citations of the references and present a brief summary of this work. Technical details and results are but may be seen in the papers cited below.

To understand waveform design for radar STAP, we had to revisit the STAP formulation from first principles and investigate at what stage of processing the waveform degrees of freedom could be used for ameliorating the effects of clutter. Toward this goal, we spent a considerable amount of time toward the STAP model and concluded that waveform design in radar STAP is only possible prior to pulse compression / matched filtering.

Therefore, a new STAP model using both fast time slow time processing was developed to aid in joint spatio-temporal waveform design. The model included effects of the noise, interference as well as, the waveform dependence of the clutter correlation matrix in fast and slow time. As a first step toward waveform design, we ignored the effect of this waveform dependence and solved a MVDR type optimization to obtain the minimum eigenvector solution. The waveform was then obtained using simple least squares. Technical details are seen in the citation below.

[1] P. Setlur, N. Devroye, and M. Rangaswamy, “Waveform Design and Scheduling in Space-Time Adaptive Radar”, In proc. IEEE Radar Conf., Ottawa, CA, May, 2013.

Continuing this work, we now enforced the waveform dependence on the clutter correlation matrix. The joint waveform and filter design problem, however, was intractable. Nonetheless, we analytically demonstrated that the optimization objective was individually convex in the waveform for a fixed filter and vice versa. This motivated us to derive an alternating minimization approach, and strong duality was shown analytically. Technical insights and results may be seen in the citation below.

[2] P. Setlur, M. Rangaswamy, ‘Signal Dependent Clutter Waveform Design for Radar STAP”, In proc. IEEE Radar Conf., Cincinnati, OH, May, 2014.

We then considered waveform design now for single sensor systems, unlike STAP, and using information theory for not just one but two waveform scheduling instants. I.e., Waveform design over two consecutive transmission time instants or epochs was the focus. The waveforms were designed to maximize the mutual information (MI) over the two time epochs. For a single epoch, maximizing the MI is equivalent to water filling. We however showed that for two epochs, the designed waveforms must satisfy two criteria. The first is water filling, and the other is that the waveforms must place energies in those spectral bands which offer maximum uncorrelated target scattering responses. The interplay of these two criteria causes the waveforms to be distinct from those designed by the single-epoch waterfilling-based systems. Comparisons of the waveforms

designed over one epoch, and over two epochs revealed a significant difference. Technical details are seen in the citation below

[3] P. Setlur, N. Devroye, M. Rangaswamy, “Radar Waveform Design with The Two Step Mutual Information”, In proc. IEEE Radar Conf., Cincinnati, OH, May, 2014.

This concludes the summary of the major contributions during this reporting period. Some of our time was also devoted toward researching aspects of optimization theory, passive radar and random matrix theory and are not reported here.

5 SOFTWARE DEFINED ARCHITECTURE-BASED COGNITIVE WAVEFORM DEVELOPMENT AND IMPLEMENTATION (prepared by Z. Wu)

5.1 Introduction

In this project, we have conducted research and development of a software defined architecture based cognitive waveform for cognitive radio and dynamic spectrum access network. Additionally, we use Universal Software Defined Radio Peripheral (USRP) software defined radio platform and GNURadio software to implement and demonstrate the developed cognitive waveform generation technology.

5.2 Software Defined Architecture based Cognitive Waveform

With the recent advances in cognitive radio and dynamic spectrum access network technologies, there is a strong need of generating cognitive waveforms that are dynamically adaptive to spectrum environment change. Given the adaptive and dynamical nature of the cognitive waveform required in cognitive radio and dynamic spectrum access network, it is natural to use a software defined architecture instead of conventional hardware approach to generate such cognitive waveforms.

Figure 1 illustrates the cognition cycle in the cognitive radio and dynamic spectrum access network. The cognition cycle contains three components: sense, lean and adapt. Firstly, the "sense" component conducts conventional spectrum sensing to sense and monitor the time-frequency environment from the cognitive radio node. Next, the "learn" component extracts important knowledge and patterns of the radio frequency spectrum such as the carrier frequency, Baud rate, modulation type, time varying pattern, etc. These knowledge and patterns are fed to the "adapt" component to adaptively adjust the waveform design to generate a cognitive waveform best suited to the current spectrum environment.

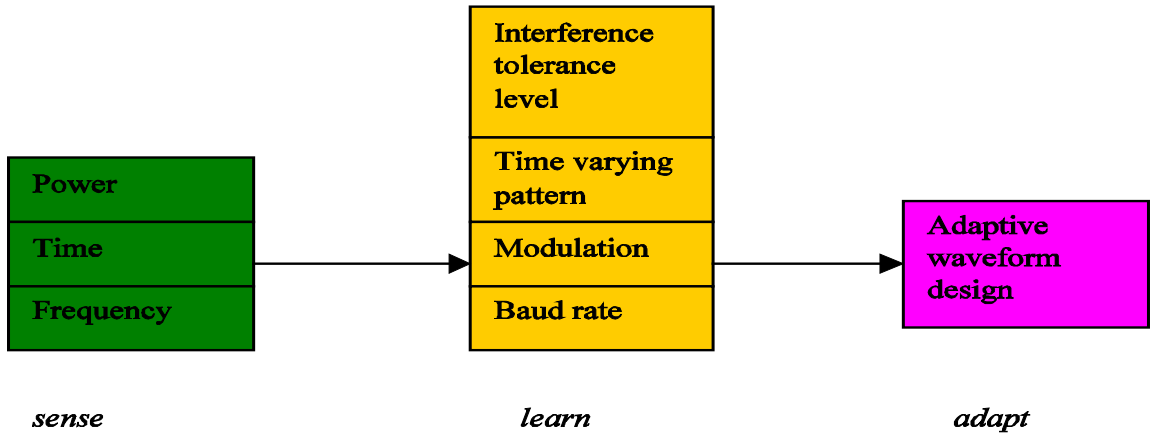

Figure 1 Cognition Cycle of Cognitive Radio and Dynamic Spectrum Access.

5.3 USRP Software Defined Radio Platform and GNURadio

Software Defined Radio (SDR) has emerged in recent years as a very useful and working concept for current and future wireless communication system design. In SDR, key components of the radio are implemented in software. Figure 2 shows a typical diagram of SDR. Take the receiver in Figure 1 as an example, received RF signal goes through the RF frontend and feeds to an analog to digital converter (ADC), then the output of ADC, the digital signal, goes into, and will be processed by, the software based communication receiver. In SDR, no complicated and expensive analog circuitry is needed to perform the transmission. On the contrary, software defines the transmitted waveforms and demodulates the received waveforms. Software radio has led the trend in the wireless communication arena to design and build wireless communication systems using reconfigurable software rather than fixed hardware.

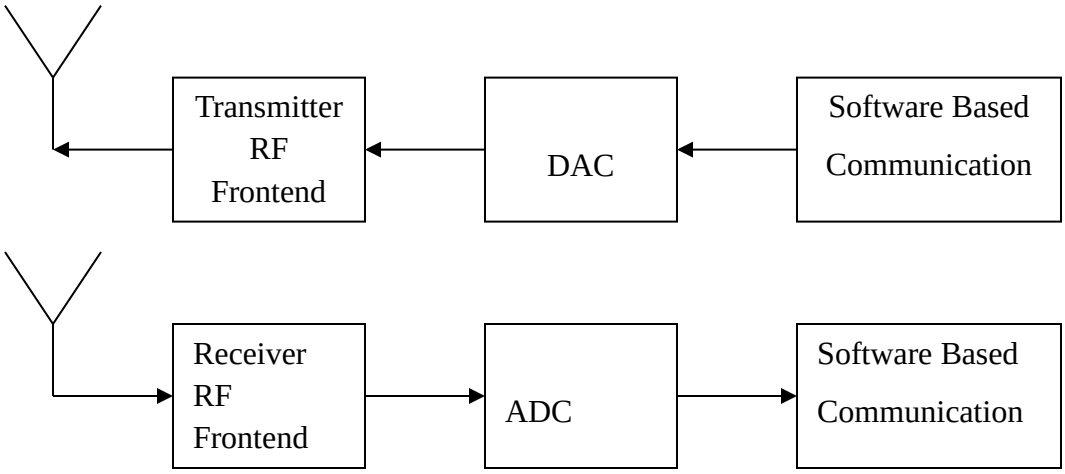

Figure 2 Typical software radio block diagram.

Given the adaptive and dynamical nature of the cognitive waveform generation in cognitive radio and dynamic spectrum access network, it is natural to employ a software defined architecture such as SDR to generate such cognitive waveforms.

We have used off-the-shelf Universal Software Radio Peripheral (USRP) developing boards that support GNU radio software for this project. The USRP is designed to allow general purpose computers to function as high bandwidth software radios. Figure 3(a) shows the SDR based experimental setup. Figure 3(b) is a picture of the USRP developing board. The USRP consists of a small motherboard containing up to four 12-bit 64M sample/sec ADCs, four 14-bit, 128M sample/sec DACs, a million-gate field programmable gate array (FPGA), and a programmable USB 2.0 controller. Each fully populated USRP motherboard supports four daughterboards, two for receive and two for transmit. RF front ends are implemented on the daughterboards. Daughterboards are designed to be easy to prototype in order to facilitate experimentation.

Current USRP transceiver daughterboards provide frequency up to 2.4GHz with bandwidth of 20 MHz and 14-bit resolution.

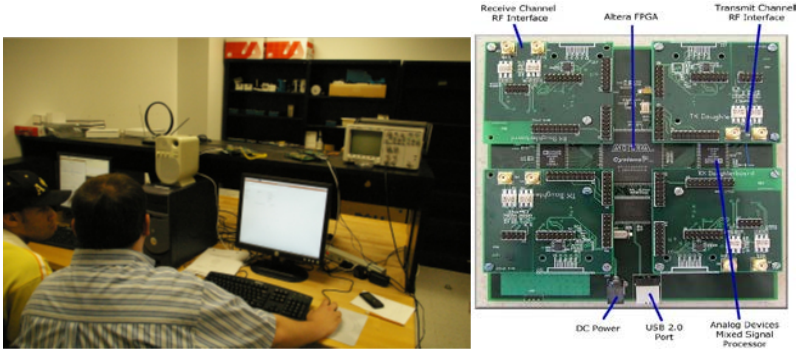

Figure 3 (a) SDR based Cognitive Waveform Generation Setup; (b) USRP software radio developing board.

5.4 SDR based Cognitive Waveform Generation

Figure 4 shows the SDR based cognitive waveform generation platform. Also shown in the figure is a wireless test and measurement system including arbitrary waveform generator, vector spectrum analyzer, wireless channel emulator, to validate the spectrum property of the generated cognitive waveform.

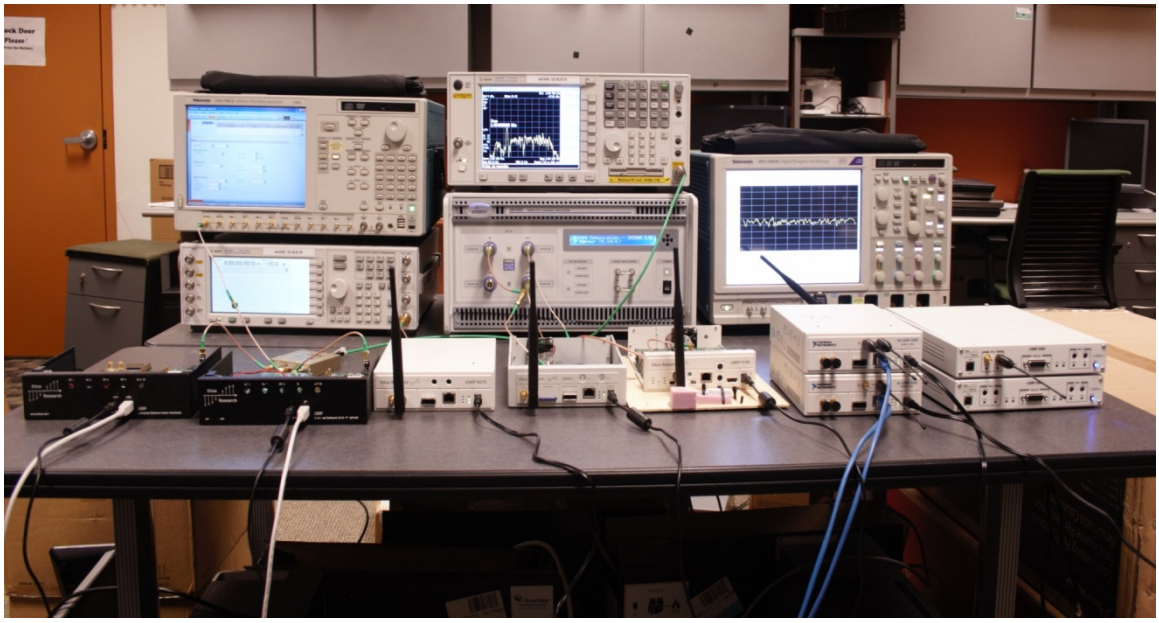

Figure 4 SDR based Cognitive Waveform Generation Platform.

Employing the SDR based cognitive waveform generation platform, we have conducted research and development of generating cognitive waveforms for different spectrum environments. Figure 5 shows the spectrum of an example of the cognitive waveform generated from the platform where no primary user is transmitting in the band of interest. Hence, the generated cognitive waveform occupies the entire band.

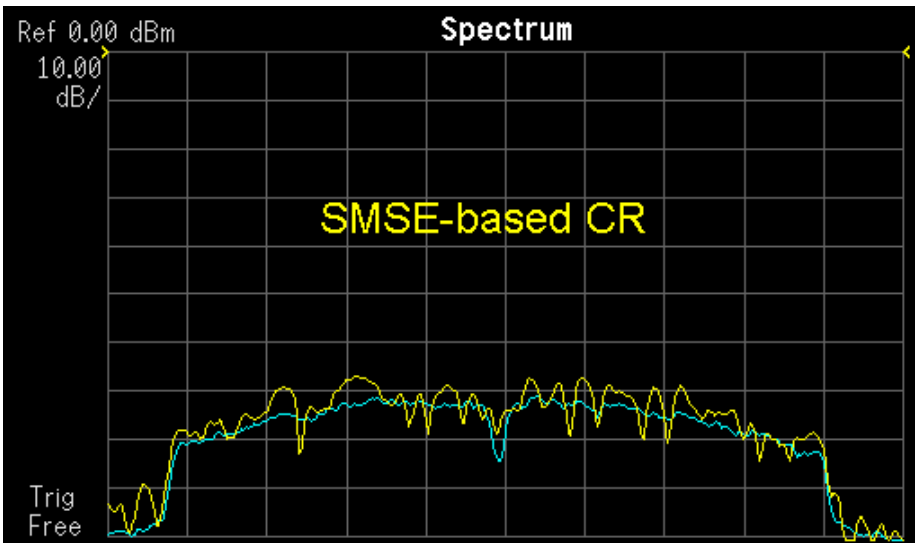

Figure 5 Cognitive Waveform Example I.

Figure 6 shows the spectrum of another example of the cognitive waveform. Now, one primary user is transmitting in the band of interest. Consequently, the cognitive waveform turns off transmission around the primary user to avoid interference to and from the primary user.

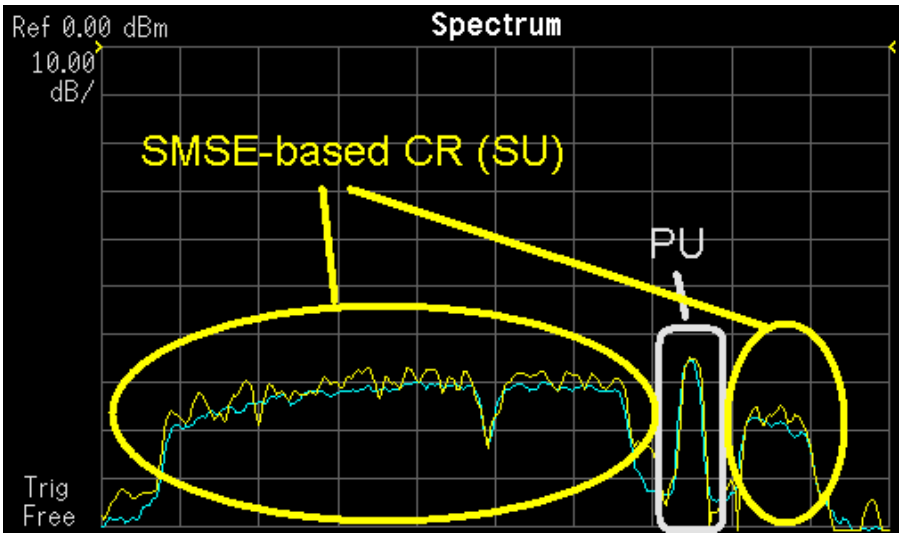

Figure 6 Cognitive Waveform Example II.

Figure 7 illustrates the spectrum of the third example of the cognitive waveform. Compared with the scenario shown in Figure 6, now the primary user has hopped to a different frequency within the band of interest. Therefore, the cognitive waveform generator automatically adjust its waveform to adapt to the new spectrum environment.

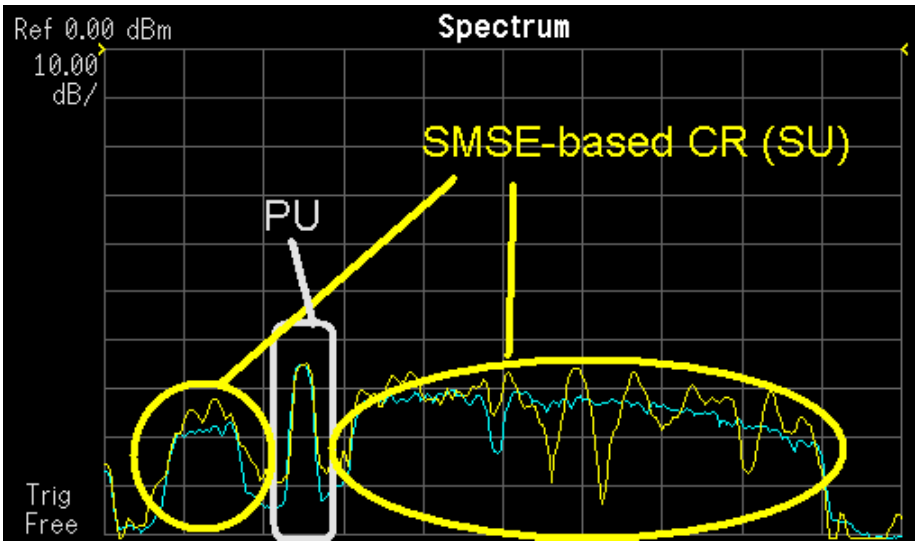

Figure 7 Cognitive Waveform Example III.

5.5 Conclusions

In this project, we have successfully developed a software defined architecture based cognitive waveform generator and implemented it via software defined radio platform. The developed cognitive waveform generator is capable of adaptively adjusting its RF parameters to avoid interference to and from the primary users that might co-exist with the cognitive radio nodes in the same band.

6 PASSIVE MULTISTATIC RADAR PERFORMANCE ANALYSIS (prepared by S. Gogineni)

There has been a growing interest in passive radar systems in the research community over the last decade because of the several merits they offer, including ease of deployment, low-cost, and non-detectability of the receivers. During the same period, the idea of distributed MIMO radar and its advantages under the coherent and non-coherent operating scenarios has been extensively studied. While passive radar systems have received increased attention operating in multistatic configuration during the last decade, there has been a lack of qualitative performance analysis of these systems. We have studied the ambiguity properties of passive multistatic radar systems using third generation universal mobile telecommunications signals (UMTS) and the fourth generation long term evolution (LTE) signals as the illuminators of opportunity. We computed the ambiguity profiles of this radar system under both the coherent and non-coherent modes. The non-coherent processing mode improves the target detection performance when compared with passive bistatic radar by obtaining spatially diverse looks of the target. On the other hand, coherent processing enhances the resolution of target localization.

The ambiguity function is an important performance metric for radar systems because it describes the global resolution performance in terms of main lobe width and side-lobe energy. However, for analyzing the local estimation accuracy, the Cramer-Rao lower bound provides a bound on the local estimation error variance of unbiased estimators in the presence of noise. Further, under certain conditions, the maximum likelihood estimators achieve the CRLB asymptotically and hence the bound can be used as an accurate measure of system performance. Since the signals of opportunity are randomly varying from pulse to pulse, we have computed modified CRLB expressions for passive multistatic radar under both coherent and non-coherent processing modes. We have demonstrated that the MCRLB is much lower for the coherent mode than the non-coherent mode thereby offering better estimation accuracy. However, note that non-coherent processing is still important in scenarios where the target induced geometry-dependent random phase-changes do not permit a phase coherent integration of the signals coming from different constituent bistatic pairs. Therefore, the choice of operating mode is dictated by the prevalent multistatic radar target model under consideration.

We demonstrated the dependence of the MCRLB results and the ambiguity function on the inherent multistatic geometry and the illuminator of opportunity. This study will facilitate in solving the important problem of optimal illuminator selection from amongst several choices. Further, we have computed the mean-squared error performance of the maximum likelihood estimators to demonstrate the validity of the CRLB for the signal to noise ratios of interest. Our research on the above mentioned topics culminated in the journal and conference publications listed in the following section.

6.1 Publications

[4] S. Gogineni, M. Rangaswamy, B. Rigling, and A. Nehorai, "Cramer-Rao bounds for UMTS-based passive multistatic radar," *IEEE Trans. on Signal Processing, Jan. 2014*.

[5] S. Gogineni, M. Rangaswamy, B. Rigling, and A. Nehorai, "Ambiguity function alalysis for UMTS-based passive multistatic radar," *IEEE Trans. on Signal Processing, Jun. 2014*.

[6] S. Gogineni, M. Rangaswamy, and A. Nehorai, "Passive multistatic radar based on long-term evolution signals," *Proc. 48th Asilomar Conf. Signals, Syst. Comput.*, Pacific Grove, CA, USA, Nov. 2014.

[7] S. Gogineni, M. Rangaswamy, B.Rigling, and A. Nehorai, "Cramer-Rao bound analysis for passive multistatic radar using UMTS signals," *Proc. IEEE Radar Conference*, Cincinnati, OH, USA, May. 2014.

[8] S. Gogineni, M. Rangaswamy, B.Rigling, and A. Nehorai, "Ambiguity function analysis for passive multistatic radar using UMTS signals," *Proc. IEEE Radar Conference*, Cincinnati, OH, USA, May. 2014.

7 OBJECT DETECTION AND TRACKING (prepared by T. Wischgoll)

7.1 Overview

This project aimed to improve detection and tracking of objects captured via different types of camera feeds. This is particularly useful in the area of surveillance. Due to the fact that a large number of surveillance feeds are typically deployed nowadays, the point is often reached were it is uneconomical and in many cases simply not feasible to have those feeds analyzed by human personnel. Instead, algorithms are needed that can detect, identify, and track objects captured within the surveillance feed and then flagged for further investigation. This project focused mostly on the tracking aspect of a detected object within such a camera feed.

There have been many proposed designs for trackers. For example the histogram of gradients, or HOG, tracker uses features from a distribution of intensity gradients, or edge directions, to form detections to use in a tracker.. Another type of tracker is a kinematic tracker that uses motion of an object to determine how the object will be tracked. The tracker used in this research is a feature aided tracker, or FAT. A FAT uses both features and kinematic metrics to track an object. The FAT used for this research is described later in the document.

The main components of the FAT used in this research are the video input device, detector, feature noise filter, and associator. The video input device is the component that is responsible for reading in the video that is going to be tracked. For this research, gray scale video is being read in by the video input device. Once the video is read in, the video stream is converted into images that can be passed to the detector. The detector takes the images from the video and forms detections. Detections used in this research are formed by using frame differencing to extract the foreground objects from the background object. The justification for the decision for using frame differencing over background modeling will be provided later in the document. The detections that are formed by the detector are then passed along to the feature noise filter. The feature noise filter will help decide which detections are likely to be moving object and which detections are likely to be noise. To determine which detections are valid the feature noise filter will used extracted features to judge if the detections are valid or not. The feature noise filter will then send the detections that belong to moving objects to the associator. The associator will then match the moving object detections with the current tracks. If there are no current tracks to associate the detections with, the associator will process a few frames before creating a new track from correlated detections. Also, if no track has matching detection over a set number of frames, the associator will terminate the track.

Typically, trackers are very sensitive devices. Any change in camera movement, or lighting, will reduce the accuracy of the tracker. A moving camera will introduce more noise since some background objects will appear to be at different location in the two frame differenced images. Changes in lighting can change the appearance of objects in an image. Shadows being casted by

a building could make tracking a vehicle more difficult. Both the camera movement and lighting will introduce more noise into the tracker. By introducing more noise, the tracker will have a more difficult time maintaining a quality track due to the noise in the detections. One of the problems created by the added noise is the multi-fragmentation problem.

The multi-fragmentation problem is when an object is assigned with two tracks instead of one track. Having two tracks on the object instead of one track reduces the performance of the tracker by increasing the redundancy. The FAME algorithm developed in this research will work on correcting the multi-fragmentation problem. To correct the multi-fragmentation problem FAME will match smaller fragments with similar smaller fragments to create larger fragments.

The goal of this project is to propose a solution to solve the multi-fragmentation problem. The proposed algorithm is meant to be ran on the feature noise filter. By running FAME on the feature noise filter component FAME is able to filter out the noise from the detections. Once the noise is filtered out, small fragments with similar features will be matched together to form a large fragment. These larger fragments can then be passed to the associator for matching. Figure 8 shows a flow chart of the FAT with the FAME algorithm developed from this research.

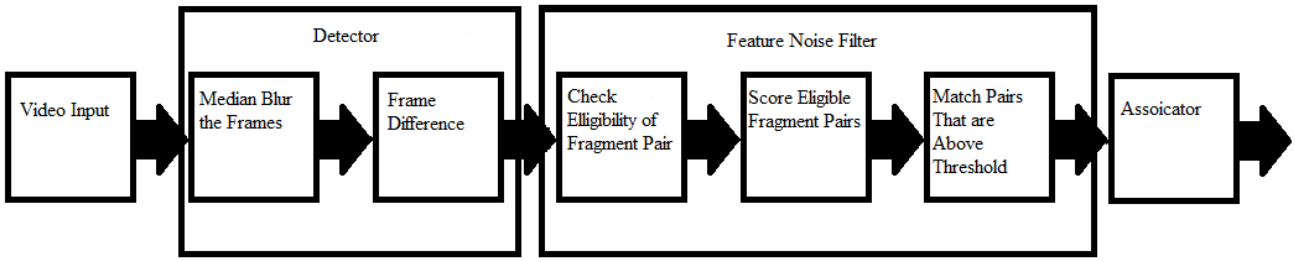

Figure 8 Flow Chart of Proposed FAT with the FAME Algorithm.

7.2 Implementation

The FAME algorithm described in this section was developed using the C++ programming language on a Linux operating system. The open source library OpenCV was also used to implement some of the computer vision and pattern recognition algorithms. The proposed FAME algorithm went through multiple test cycles to determine which features would yield the best results. This chapter contains information that goes into great detail about the feature noise filter described in Figure 8 earlier in the document. The main steps to describe the functionality of FAME are: check eligibility of fragment pairs, score eligible fragment pairs, and match fragments pairs. FAME does contain three user defined parameters.

The first user defined parameter is the largest allowable pixel distance between a fragment pair. The distance between two fragments is measured from one fragment's centroid to the other

fragment's centroid. If a fragment pair's Euclidean distance is below the pixel distance threshold they will be considered for matching. The fragment pair will not be sent to the matching phase if their Euclidean distance is greater than the pixel distance threshold. The second user defined parameter is the largest allowable fragment feature score of a fragment pair. Fragment pairs with a low score are considered to be a close match. If the fragment pair has a very high score, then the fragment pair is not a match. The third user defined parameter is a minimum allowable gradient pixel intensity used in the post-processing. If a fragment pair wants to pass the post-processing step the area between the two fragments must have a gradient pixel intensity higher than the allowable gradient pixel intensity variable.

The FAME algorithm for the feature noise filter expects to receive a binary detection image from and a gray scale image from the detector. The binary detection image contains the foreground object detections from the detector component. The gray scale image is used for feature calculations on the fragments. In addition to the feature calculations, the gray scale image is used for the post-processing gradient calculation. FAME assumes that there are no major changes between the current and the previous frame. So either the current or previous gray scale frame can be passed to FAME along with the binary detection image.

7.2.1 Checking eligibility of fragment pair

FAME begins by extracting the fragments from the binary detection image that was passed to the feature noise filter from the detector. Once the fragments are extracted every fragment pair distance will be checked against the distance threshold. If a fragment pair distance is less than the distance threshold they will be passed along to the next section of the feature noise filter. The following sections describe the tools and concepts used to complete the check eligibility of fragment pair section.

7.2.2 Finding Contours

Once the binary image is passed to the feature noise filter FAME will use the openCV findContours routine. The purpose of the findContours routine in FAME was to find the location of the fragment's from the binary detection image. The openCV findContours routine is a border following routine that finds and marks all the foreground objects in the image. When finding the fragments, findContours stores the locations of the points used to outline the fragment. The points are stored in (x, y) coordinates. The function findCountours has the ability to create a hierarchy of all the fragments in the image. Any contour inside of the image is on the first level of the hierarchy. It is possible that a contour on the first level can have a hole that contains another contour. This contour inside of the first hierarchy is then placed on the second level of the hierarchy since the contour is inside of another contour.

7.2.3 Calculating distance between fragments

After the fragments have been extracted using findContours the distance can be calculated between each fragment pairs. FAME uses the centroid of each fragment to calculate the distance

between the fragment pair. The openCV findContours method does not contain the centroid for each fragment. In order to find the centroids of the fragments, FAME will use first order moments. The first order moments will return the average x and y value to be used as the centroid for the fragment. Now the Euclidean pixel distance can be calculated between each fragment's centroid. Once this distance is calculated. The fragment's distance will be checked against the distance threshold. If the distance is less than the threshold, then the fragment pair can move on to the next phase. However, if the fragment pair's distance is greater than the threshold the fragment pair will no longer be considered an eligible fragment pair for matching.

7.2.4 Scoring eligible fragment pairs

The scoring section gives each fragment pair a score of how likely a match they would be. Each fragment pair score is based off a sum of normalized features. For this project the features were normalized to be between 0 and 1. With 0 meaning the fragments are very similar and 1 meaning the fragments are very different. In addition to the two fragments being eligible for feature scoring, the area between the features can be used for feature calculation. A separate routine was created for extracting the area between the fragments.

7.2.5 In-between Fragment Calculation using Arc Tangent Function

The new in-between fragment calculation uses the arc tangent function to find the angel that the in-between fragment area is rotated. The fragment area will be rotated when the two fragments are diagonal from one another. This in-between fragment calculation using arc tangent still uses the findContours bounding box routine to extract the four points around each fragment. The distance is calculated between the four points of one fragment to the other fragment. The two pairs of points with the shortest distance are then used for the in-between arc tangent fragment calculation. The main difference between this in-between fragment calculation and the previous in-between fragment calculation is that in this case it does not create new points like the previous in-between fragment calculation. Instead, this in-between fragment calculation creates a rotated bounding box from the two pairs of closet fragment points. This bounding box is then rotated using an angle determined by the arc tangent function. The angle used by the arc tangent function is dependent on how diagonal the two fragments are.

The arc tangent in-between fragment function uses four points to define the rectangle of the in-between fragment. The four points used to define the rectangle are the two pairs of the points from fragments f1 and f2 that have the smallest distance. From the four points the closest and farthest point from the origin are determined. The origin is defined by where in the image the location is (0,0). In the OpenCV library, the origin of the image is located in the upper left corner. Figure 9 below shows a graph with the four points representing the rectangle for the in-between fragment. Point P3 and P1 come from fragment f1 and points P4 and P2 come from fragment f2.

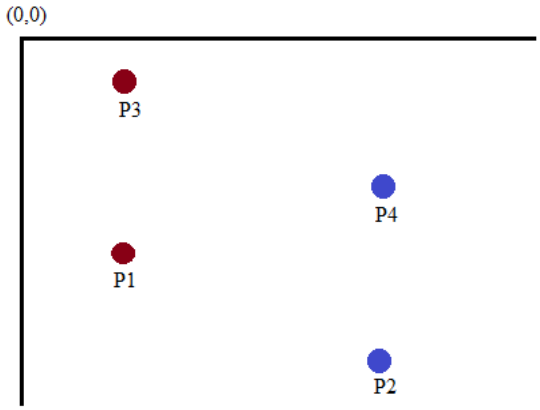

Figure 9 Graph Showing the Four Points used to Represent the Area of the In-between Fragment.

Once the closest point to the origin is determined, the farthest point is calculated. The farthest point is determined to be the point opposite of the closest point. If the rectangle used to represent the rotated bounding was split into two triangles, the opposite point from the closet point would be the farthest distance away based on the Pythagorean theorem. The opposite point would lie on the hypotenuses, making the opposite point farther than the two adjacent points with respect to the closest point. Figure 10 below shows the in-between rectangle being split into two right triangles.

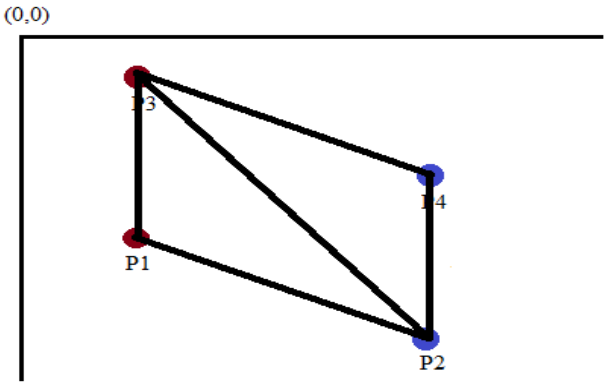

Figure 10 The Four Points from Figure 9 being Split into Two Triangles.

Using the closest and farthest point, the rotation angle of the in-between fragment was calculated. The in-between fragment could then be calculated using the four points and the rotation angle. Using the rotation angle prevented overestimating pixel in the in-between fragment. Instead of having to create a new set of points, like in the previous in-between fragment calculation, the rotation angle allowed the tangent in-between fragment calculation keep the four points from the two fragments. By not having to create new points, the tangent in-between fragment calculation did not suffer from overestimating the area of the in-between

fragment. Below the two red rectangles represents a pair of fragments. The rotated green rectangle represents the in-between area calculated in this function. However, in order for OpenCV to process the pixels in the green rectangle a bounding box must be placed around the rotated rectangle. In Figure 11 the bounding box is represented in yellow. All the pixels in the bounding box will be used for the pixel estimation. The bounding box in this section contains less pixels than the bounding box in the previous in-between section. Therefore the bounding box in this section will give a more accurate representation of the area between the two pixels.

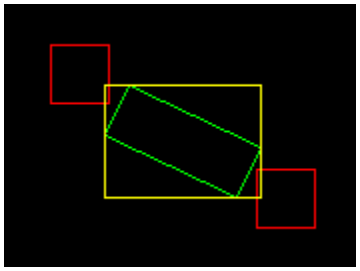

Figure 11 The Final Result from the In-between Fragment Calculation.

7.2.6 Scoring Fragment Pair

The scoring of the fragment pair is used to represent how likely a fragment pair is to be a match. All the feature values used in the score are normalized between 0 and 1. A score close to 0 means the fragment pair is a close match. That in turn makes scores close to 1 a non-match. The equation below describes the formula used to calculate the score.

Equation 1

The scoring equation is very flexible since one or more features can be used to determine the likelihood of a fragment pair. During the testing of FAME, different combinations of features were used in the score calculation. One such combination of features were: hu moments, haralick features, and eccentricity. If a score is lower than the user defined score threshold value, the fragment pair is eligible for matching.

7.2.7 Match Pairs that are above threshold

To match a pair of fragments, a line is drawn to connect the two fragments together. The line used to connect the fragments goes from one fragment's centroid to the other fragment's centroid. If a fragment is shared by multiple pairs then the fragment will contain multiple lines connecting itself to other fragments. By allowing a fragment to connect to a multiple of other fragments there is a chance that two close fragments pairs could just become one large fragment. However, if multiple fragments were not connected together a large fragment consisting of three smaller fragments would never be created. The post-processing gradient checking was created to ensure two close fragments would not be matched together even if their threshold was below the

allowable threshold value. By matching the fragments together two or more small fragments turn into one large fragment. For example two small fragments could represent the front or rear of a bus. By matching the two fragments together the bus's front gets matched with the rear to create the entire bus.

7.2.8 Post Processing

Before any matched fragment pairs are passed along to the associator FAME will double check if the match is correct or not. To ensure the fragments are a correct match FAME uses an edge image created by the absolute gradient magnitude from Sobel operators. The more defined edges in the gradient image will have a higher intensity than any non-edges. Knowing this, FAME can compare the location between the fragment's centroid in the foreground image to the location in the gradient image. If the area between the two centroids have a high enough intensity, FAME will allow the fragment pair to pass along to the associator. However, if the intensity is to low, the fragment pair will not be passed to the associator. Figure 12 and Figure 13 below show what FAME is looking for when the matched fragment pair is compared to the absolute gradient magnitude edge image.

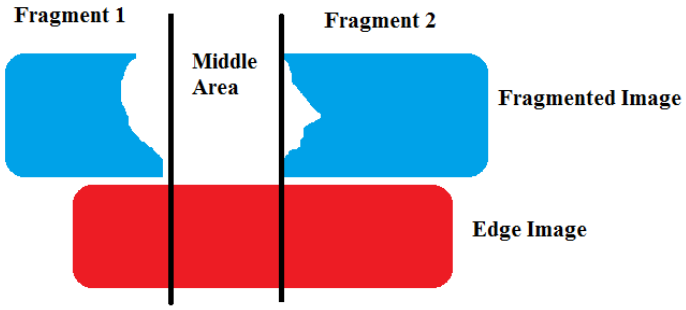

Figure 12 Fragment Pair that Passes the Post-processing Check.

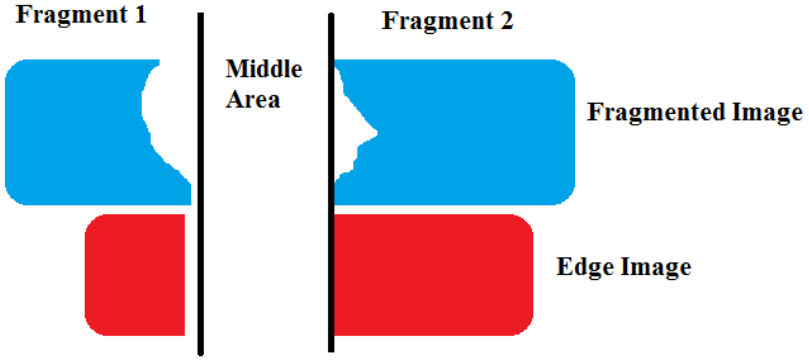

Figure 13 Fragment Pair that will not Pass the Post-processing Check.

7.3 Results

When conducting the experiments on FAME choosing which data to use in testing was very

important. Each data set had to contain at least two cars of any size or color. These multiple cars had to have the ability to drive close together, change speed, and direction. By having multiple cars, FAME was tested on how well the fragments from the cars were matched to the correct corresponding car. Also, the data used to test FAME had to come from a moving camera. The data from the moving camera tested FAME's ability to remove noise from the detection image that might be caused from camera movement. The program COMPASE Tracker Evaluation Software Suite (CTESS) was used to test how well FAME preformed on the FAT. Testing the results from the FAT using CTESS required two sets of data.

The first set of data was track points generated by the FAT. These track points were used to represent the location of the object being tracked by the FAT in (x, y) coordinate space. The second set of generated data was the truth points. The truth points are the actual locations of the moving object in (x, y) coordinate space. Once CTESS has those two sets of data, a frame from the track points was compared to a frame from the truth points. Since CTESS compares frame-to-frame from each data set it is very important that the track points and the truth points are extracted at the same frame rate. One way CTESS analyzes the data is by checking if the track points are relatively close to the truth points based on a pixel distance threshold. If a track point is within the pixel threshold distance of the truth point, the track point will be matched to the truth point. Also, if two track points are close to a single truth point, the two track points will be matched to the truth point. Having the two track points matched to a single truth point is sub-optimal since that will increase the redundancy**.**. If there is no truth point within the pixel threshold of a track point that track point will be marked as spuriousness as defined below. The following terms will be used to describe the performance of the FAT with the FAME algorithm**.**

Purity: how many tracks were correctly associated with the truth point.

Completeness: how many tracks were associated with a truth point.

Redundant: how many tracks were associated with each truth point. There should only be only one track per truth point. If more than one track point is associated with the truth point, the tracker will suffer from the multi-fragmentation problem.

Spuriousness: how many false alarms were in the track points. A false alarm is generated when there are no truth point to be associated with the track point.

Experiments were conducted to see how much FAME would improve the performance of the FAT using different test scenarios. The FAT with FAME will be considered improved if two criteria are met. The first criterion is that the FAT with FAME must have a higher completeness and purity than the FAT without FAME. By meeting the first criterion, that would mean that more of the tracks were match to the truth points using the FAT with FAME instead of the FAT without FAME. The second criterion is that the redundancy and spuriousness must be less on the FAT with FAME compared to the FAT without FAME. By reducing the redundancy and

spuriousness, the FAT with FAME will show the ability to have less incorrectly matched tracks than the FAT without FAME. The experiment used five different test scenarios.

The test scenarios contained different cars that needed to be tracked in the video. The cars are performing different maneuvers, such as traveling close together and making a turn, one car passing the other, taking a U-turn and stopping after a while. Figure 14 shows a sample scenario. The three tests applied to each scenario were the FAT without FAME, FAT using FAME with a scenario global score and gradient value, and FAT using FAME with a scenario tuned value. The FAT with a scenario global value means that for all the experiments the same score and gradient threshold were used. For these experiments the global score being used was 0.35 and the global gradient intensity being used was 20. The FAT using FAME with a tuned scenario score and gradient means that each test scenario used a different score and gradient threshold. The global and scenario dependent values were tested to show that even if FAME can be specifically tuned for a data set or that a score and gradient value can be found to accurately test multiple data sets.

7.4 Evaluation

In all of the test scenarios, the FAT with FAME out preformed the FAT without FAME. The FAT with FAME had a higher completeness and purity than the FAT without FAME. Also, the FAT with FAME had the lowest redundancy and spuriousness. There are two main reasons why the FAT with FAME outperformed the FAT without FAME. The first main reason is the median filter applied to the current and previous frame before the frame differencing helped remove some of the added noise from the camera movement and frame extraction. By removing the added noise there was less noise generated fragments to be uses in the matching phase of FAME. The second reason why the FAT with FAME was able to outperform the FAT without FAME was the matching of the fragments.

Figure 14 Frame from Test Experiment Video.

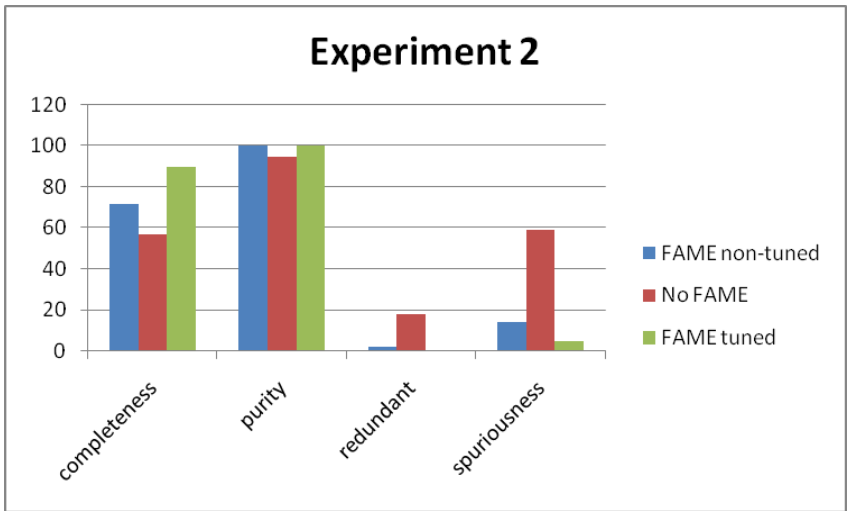

Figure 15 Comparisons of Results from a Representative Experiment.

By matching fragments that share similar features, spuriousness and redundancy decreased and the completeness increased. The reason why redundancy and spuriousness decreased was that the two smaller fragments were matched to create a larger fragment that would be passed along to the associator. Since the two small fragments were matched together there were less fragments to be matched to a truth point. Having less fragments for matching helped reduce the spuriousness and redundancy. The larger fragment made the associators job easier since there is only one large fragment to match with the previous track. If there were two small fragments, the associator would then have to decide which fragment to associate with the current track and what to do with the second fragment. Even though the FAT with FAME is an improvement, FAME still had a hard time tracking the parked cars in two of the experiments.

Tracking parked cars is one of the hardest objects to track for any tracking algorithm. Since the FAT used in this project requires motion to generate tracks, tracking any non-moving object becomes a challenge. Once the cars are parked they appeared to be part of the background to the FAT since they were not moving. Since the cars were not moving, their position never changed in the current and previous frame. By having no major changes in the current and previous frame, the frame differencing had a difficult time extracting any meaningful foreground objects. The FAT with FAME was able to track the parked cars in one of the experiments since a track was generated before the cars stopped. Once the cars stropped, the track was able to stay on the parked cars by matching the small detections calculated by the frame differencing due to the cameras movement. However, if the cars were already parked no tracks could be generated until the cars started to move. However, specifically tuning the variables did slightly help improve FAME's results in some of the scenarios.

Special tuning of the results helped in one experiment when FAME had to track cars that started moving. By increasing the gradient threshold the fragment from the two cars did not join to

create one giant car. During testing, FAME had a hard time matching fragments to cars that were really close to one another. Being really close is defined in this case as the allowable distance used by the two fragments intersecting one another. Therefore, the gradient check was developed to remove the incorrect fragment match from the close fragments. However, tuning the variables did not significantly help for all the experiments. The reason why tuning the variable to each scenario did not yield significant improvements compared to the global variable was due to the fact that the global variables were already set to an optimal value. Also, the tuned values were very close to global variable values. Therefore, the global variables and tuned variables had very similar results. The main reason why tuned variables were compared to global variables was to show the ability of FAME to use the same variables over different data sets and still get better results than the tracker without FAME.

8 MACHINE LEARNING FOR ATR (prepared by M. Rizki)

Under this task, a number of undergraduate and graduate students conducted research in concert with Wright State faculty and AFRL mentors. Each student was responsible for developing a working understanding of a research problem relevant to the Air Force and then working with their AFRL mentor to design and implement a software system to address the problem. The accomplishment of the students are summarized below.

Andrew Profeta learned to the Torch and CAFFE neural network frameworks as well as some of the basic principles of radar. He participated in the summer ATR center, and helped setup laboratory computers with operating systems and software dependencies. He also implemented a neural network framework that successfully classified radar. This research formed the basis for his Master's thesis that is in progress.

Tyler Highlander implemented an Overlap and Add (OaA) technique to extend convolutional neural networks (CNNs). To accomplish this task, he did a review of the literature on CNNs including a review of a number of the existing software implementations of CNNs. He implemented OaA in CAFEE, conducted an extensive series of experiments as part of his Master's thesis research and published the results in the British Machine Vision Conference. As a result of this research, he demonstrated that OaA can speed up CAFFE from 60 seconds per 100 iterations to 11 seconds for certain layer sizes. This represents a significant reduction in the time complexity of the computation. Tyler Highlander has entered the Computer Science and Engineering PhD program and is continuing to work with his Air Force mentor.

Ryan McCoppin conducted research conditioning multi-layered neural networks for pattern recognition tasks using deep learning (DL). The DL conditioning uses un-supervised learning techniques which do not require labeled training samples. The neural networks are conditioned one layer after another with one conditional layer clamped and acting as input for the next hidden layer. Experimental designs in DL provide a means for evolving weights so they become sensitive to the statistical structures in the unlabeled sample images. The preferred technique uses auto-encoders which employ sparsity constraints on the hidden layer and attempt to reconstruct the clamped input layer from the reduced hidden layer representation. A number techniques for reducing the activation levels in the hidden layer were also studied. Ryan completed his Master's of Science degree in Computer Science.

Ashley Coleman conducted research that explored several different dimensionality reduction techniques including diffusion maps, Isomap, kernel PCA, PCA, MDS and LPP; to determine the type of features exploited by each technique. She applied these techniques to a dataset of 10 military vehicles. She also worked to develop a survey instrument that can be used to determine what features human would extract from the dataset. The goal of the research was to compare the results of feature selection using machine learning techniques with handcrafted solution developed by humans. Ashley is using this research as part of his Master's thesis project.

Jacob Hewitt is developing software tools and systems to support video analysis. He is using the Nvidia Jetson development board to capture images via a USB 3.0 camera. He is leveraging the hardware encoder of the Jetson board coupled with metadata to create a data stream to send from a UAV to the ground station. The goal is to move some of computationally intensive processing directly into the UAV to reduce data transmission to the ground station. Jake is working to complete his BS in Computer Science.

Colin Taylor conduct research on various types of image feature detectors including the HOG based Maximum Margin Correlation Filter. He applied these techniques to a variety of image data sets relevant the Air Force. Colin is completing his BS in Computer Science.

Alexandra Hildenbrant conducted research on color detection and matching. She was able to demonstrate that the best method of color matching depend on the specific color detected. For instance, when using the HSV color model for matching between the template and test images, after filtering by hue, colors can be filtered by saturation, value, or both. For the color red, filtrating by saturation tends to exclude too much color, while value does not filter enough color. For the color blue, saturation works much better than the value. The results of this study suggest that target recognition systems using HSV color models should filter mainly by value of saturation. Alexandra is completing her BA in Theatre and BA in Computer Science. She has been hired as full-time employee by AFRL/RYAT.

9 DEPLOYABLE LOW POWER CARBON NANOTUBE SENSORS (prepared by S. Ren)

9.1 Program Overview

WSU employed post-doctorate researchers to work with Air Force Research Laboratory (AFRL) technologists to fully design, build, and characterize the interface from an AFRL sensor material to a device. Collaboration between AFRL and Wright State University (WSU) brought the materials knowledge and requirements from the former to the interface design and integration knowledge of the later. Component level testing occurred at WSU as we refined the device architecture. This was done in close partnership with AFRL. Frequent visits occurred to discuss data and the way forward as we overcame many technical obstacles. Joint participation in key tests was also necessary so the components were integrated into a final product (and demo) that meets the original needs. This collaboration is important for the particular project being funded as well as to establish a more lasting relationship between AFRL, industry in the Greater Dayton area, and WSU. In addition, WSU provided students, post-doctorate researchers, and other visitors with educational and career opportunities that strengthened the next generation of scientists and engineers for sensing applications that contributes to the Air Force and current research societies.

9.2 Task Overview

The initial task of this pilot program was to review the data obtained from AFRL for carbon nanotube (CNT) sensor characterization in Chapter 8.3 and define the CNT analysis system as well as establishing the interface CMOS chip and PCB board specification in Chapter 8.4.

The architecture for translating the CNT sensor resistance to voltage is developed with transistor level schematic and layout designs in Chapter 8.5. This also includes the discussion on the analog-to-digital convertor (ADC) and the final full CMOS chip layout used for fabrication. The completed read-out integrated circuit schematic and layouts are simulated and evaluated against the reference AFRL data set in Chapter 8.6.

The PCB board design interfacing the nanotube sensor, voltage controller, and the readout integrated circuit is discussed in Chapter 8.7. The final design for phase I has exceeded the original design specifications and this allowed wide current detection ranges for different sensor profiles, such as the zinc oxide (ZnO) gas sensor. The final fabricated CNT analysis system is interfaced with the ZnO sensor and shows favorable current measurement results in Chapter 8.8. The final chapter of this report documents ideas and improvements for further possible research work in future collaborations.

9.3 Carbon Nanotube Data (AFRL) and Characterization

The AFRL carbon nanotube is illustrated by Dr. Sang Nyon Kim in Figure 16. Fixed gate and source-to-drain voltages are applied to the CNT sensor to measure the current flow through the sensor. Two sets of CNT measurement data were provided for characterization.

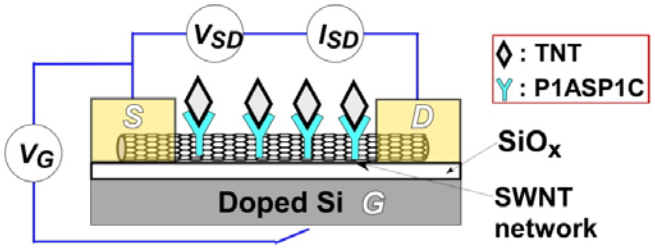

Figure 16 Carbon Nanotube Model.

The first measurement data illustrated in Figure 17 maintains the source-to-drain voltage to 0.2 V while varying the gate voltage from -20 to 20 volts. This established the relationship between source-to-drain current and gate voltage.

The second measurement data illustrated in Figure 18 maintains the gate voltage at a fixed value while varying the source-to-drain voltage from -1 to 1 volt. Various results are provided on the same plot for a subset of fixed gate voltage values. This plot established the relationship between source-to-drain current and voltage. The two measurement data seem to be from different batch of CNT devices since no data correlations can be inferred from Figure 16, Figure 17, and Figure 18.

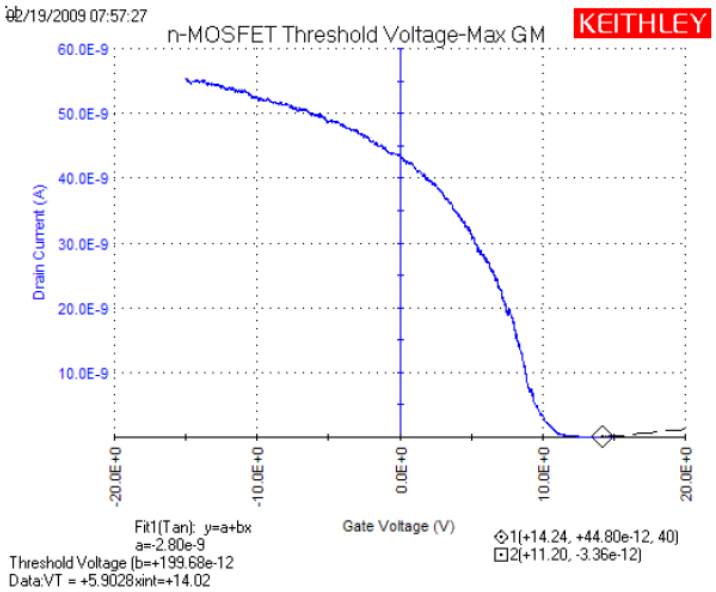

Figure 17 Source-to-Drain Current Versus. Gate Voltage.

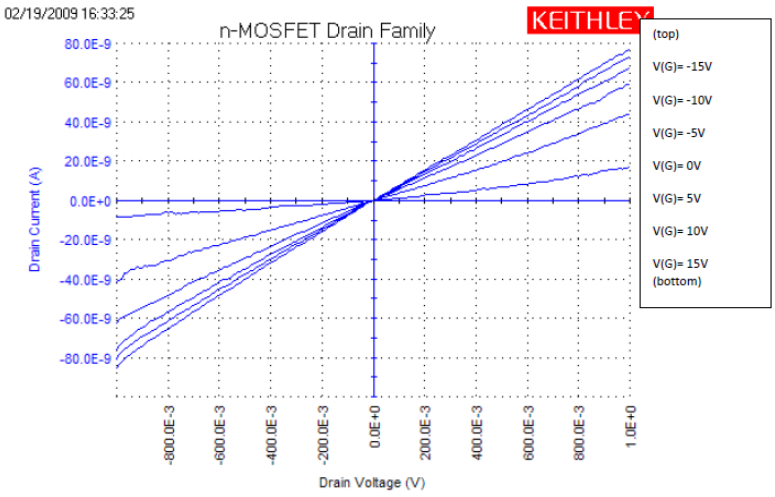

Figure 18 Source-to-Drain Current versus Source-to-Drain Voltage.

Using the data plotted in Figure 18 for various gate voltages, the source-to-drain current (I_{SD}) and voltage (V_{SD}) pairs are obtained from the recorded excel data sheet.

The I_{SD} values are obtained at V_{SD} voltages of 0.21, 0.31, and 0.41V. This is repeated for gate voltages at -15, -10, -5, 0, 5, and 10 volts. The associated current and resistance values are estimated using Ohm's Law in Eq. (3.1) and tabulated in Table 4 and 5.

$$V = IR \Rightarrow R = V / I \qquad \textbf{Equation 2}$$

Table 6 Expected Source-to-Drain Current across Sensor (AFRL Reference) [nA].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	21.4871	20.6917	19.2575	17.8825	14.9956	8.6218
-0.31	31.7354	30.5019	28.4307	26.4777	22.0543	12.9768
-0.41	41.9993	40.3136	37.6433	35.0434	29.3153	16.9029

Table 7 Effective Sensor Resistance across Source-to-Drain (AFRL Reference) [MΩ].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	9.308	9.666	10.386	11.184	13.337	23.197
-0.31	9.453	9.835	10.552	11.330	13.603	23.118
-0.41	9.524	9.922	10.626	11.414	13.645	23.665

9.4 System Requirement and Specification

Based on discussions with AFRL researcher, Dr. Sang Nyon Kim, the goal is to determine the current through CNT by maintaining a fixed voltage across the source and drain terminals (for example 0.2V) while varying the gate voltages at 1 millisecond to 10 minute intervals. A conceptual waveform showing the expected inputs and outputs of CNT is shown in Figure 19.

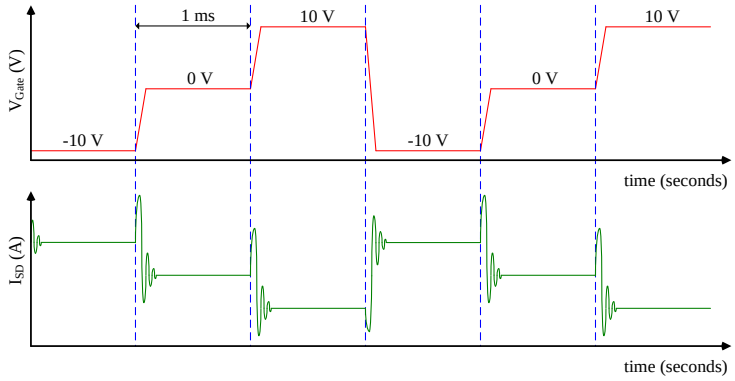

Figure 19 Conceptual Input and Output Waveforms.

Based on the above waveforms, the initial system requirements are defined. The gate voltage of CNT is varied at specific time intervals while the source-to-drain voltage is maintained close to a desired fixed value. The output current of CNT is observed and analyzed using analog and digital circuitry or directly as an analog value.

A top level system is developed to with respect to the above specifications, shown in Figure 20.

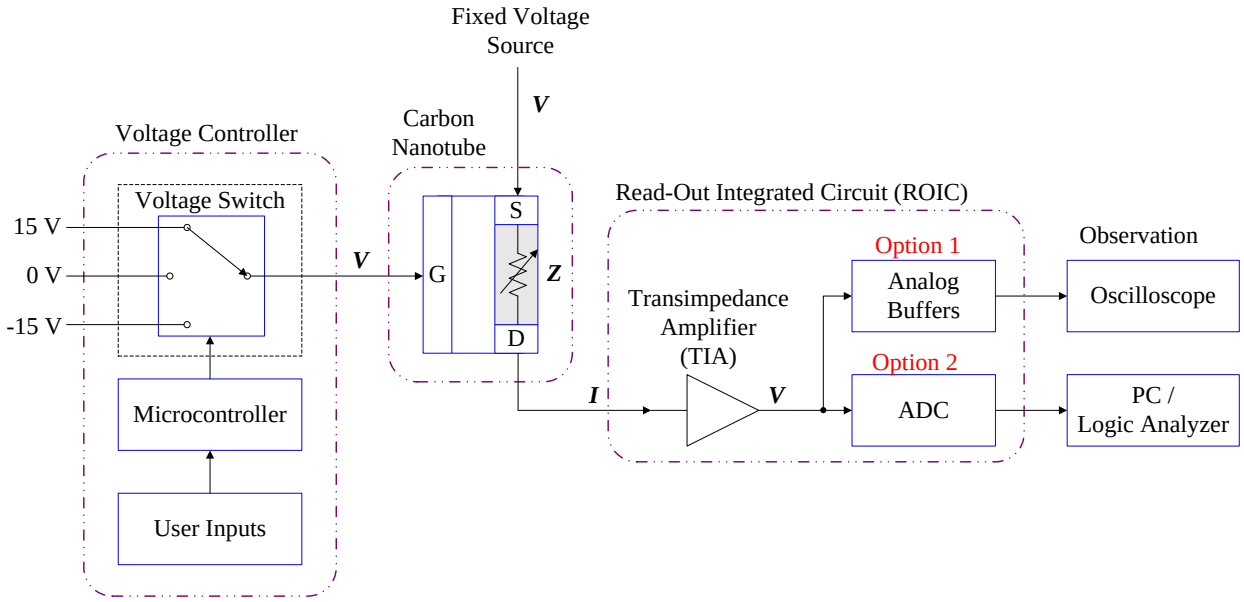

Figure 20 Overall CNT Analysis System.

Voltage ranges greater than 1.8 V are not supported by current low-power CMOS processes since it will damage the analog and digital design circuitry, thus an off-chip *voltage controller* will be needed to automatically supply the different gate voltages required for CNT. The microcontroller will determine the duration for a given gate voltage based on the user inputs. The user inputs may be configured via push buttons or dip switches to control the time period. The voltage switch is currently limited to three input voltage values, but it may be expanded to include additional voltage inputs. The *voltage controller* will be designed using commercial-of-the-shelf (COTS) parts to reduce the hardware design overhead. This portion of the system is completed with the design of the test fixture in detailed in Chapter 8.7.

The microelectronic *read-out integrated circuit (ROIC)* is based on IBM (CMRF7SF) technology for high performance complementary metal-oxide-semiconductor (CMOS) applications. The technology supports 1.8 V mosfets with minimum feature size of 0.18 μm. This fabricated chip will provide the conversion needed to analyze the voltage, current, and resistance relationships of the CNT utilizing both analog and digital post processing techniques.

Additional modifications to the overall CNT analysis system may be required in the future to synchronize the communication between the *voltage controller* and *ROIC* to match the gate voltage pulse times with the output data needed for analysis as shown in Figure 19.

9.5 Design of Read-Out Integrated Circuit

The components of the read-out integrated circuit (ROIC) consists of a trans-impedance amplifier (TIA), analog buffers for external oscilloscopes, and an ADC for future digital post processing algorithms. The components associated with TIA are illustrated in Figure 21.

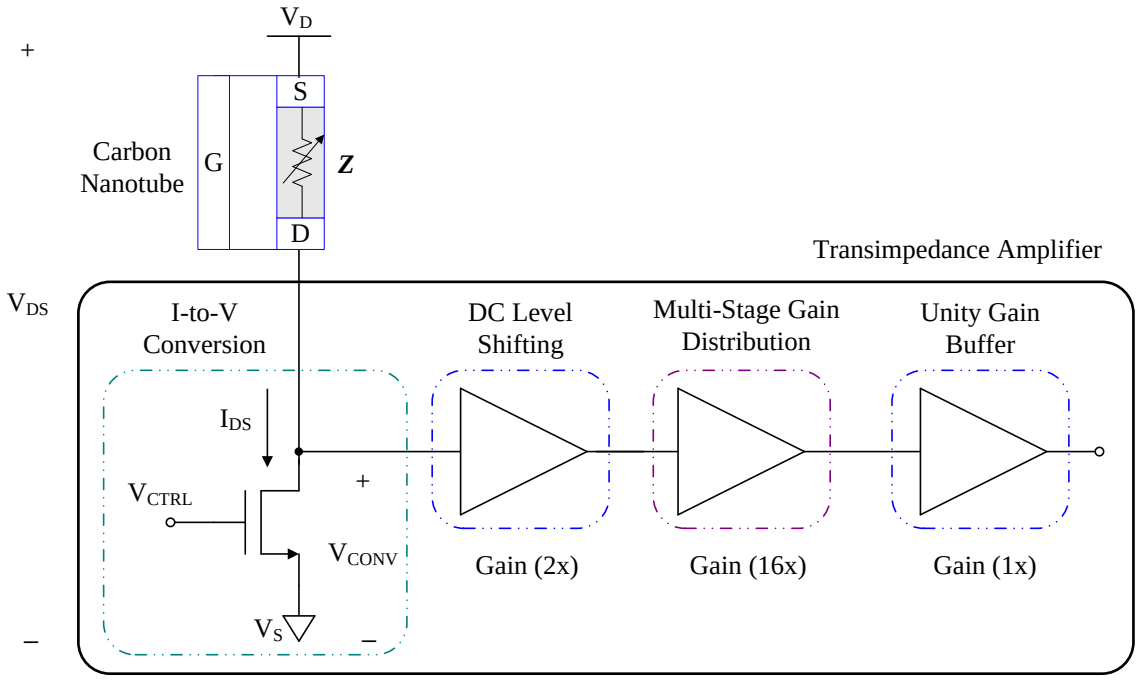

Figure 21 Trans-Impedance Amplifier.

The TIA starts with a current-to-voltage (I-to-V) conversion. A unity gain buffer is inserted after I-to-V conversion to prevent feedback currents from gain stages feeding into the sensor. Multiple stages of amplifiers are needed to amplify the sensed voltage signal for analog-to-digital conversion. Outputs from all the stages of the trans-impedance amplifier are available for the user to measure in the finished device.

9.5.1 Current-to-Voltage Conversion

The architecture for I-to-V conversion is based on the concept of voltage divider, illustrated in Figure 22, where the resistor is implemented as an active transistor M_{CONV}, shown in Figure 23. All the results presented in this section are based on the use of advanced CAD tools using a design kit and models that are matched to the 0.18 CMOS process.

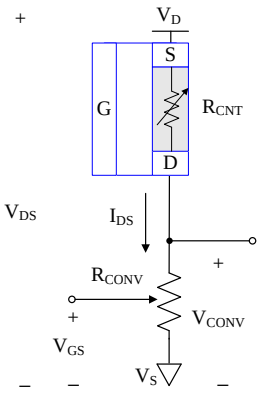

Figure 22 I-to-V Conversion (Resistor).

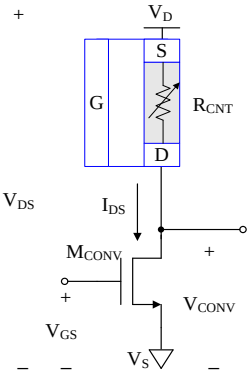

Figure 23 I-to-V Conversion (Active Transistor).

The main advantage of this design is the current will flow directly from the V_D to V_S terminals, no DC current will flow to and from the unity gain buffer due to the inherent capacitor at the gate terminal of the transistor. The voltage V_{CONV} is induced by the load resistor R_{CONV}, the relationship between I_{DS} and V_{CONV} is shown in Equation 3.

$$V_{CONV} = \left(\frac{R_{CONV}}{R_{CNT} + R_{CONV}} \right) V_{DS} \qquad \textbf{Equation 3}$$

Concern with this implementation is the slow settling time before a stabilized voltage value is present at the output. This is an issue for high performance signal acquisition systems operating in MHz (million samples per cycle) region. For the current specification of varying gate voltages every 1 ms, the active transistor implementation in Figure 23 operating in the linear region (non-saturation region) is sufficient.

An obvious observation is the inquiry of using an active device (transistor) over a passive device (resistor). During the CMOS fabrication process, process variation will cause the resulting resistance to differ from the one intended, which will lead to erroneous results in the subsequent stages. However with the usage of active transistor M_{CONV}, the resistance value may be adjusted via a control voltage V_{GS}. The on-resistance of an active transistor operating in the linear region is defined in Equation 4,

$$R_{CONV} = \frac{L}{\beta W (V_{GS} - V_T)}, \; V_{GS} > V_T \textbf{ and } V_{DS} < V_{GS} - V_T \qquad \textbf{Equation 4}$$

where W and L are the width and length of the transistor. V_{GS} is the amount of voltage required to turn the transistor ON with respect to the threshold voltage V_T. V_T is the minimum amount of voltage required to create an inversion layer between the gate and substrate of the transistor, a channel is then formed for conduction of electrons between and source and drain terminals

determined by the strength of the gate voltage. The β term is a function of electron mobility (for n-channel devices) and oxide thickness. This implementation has an advantage over regular resistors since the resistance value may be controlled using an external voltage V_{GS} to offset the erroneous resistance values caused by process variations. The preliminary resistance for M_{CONV} is 1 MΩ, with a V_{GS} of 0.9 V.

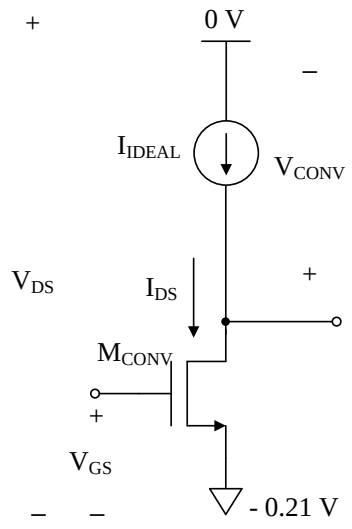

Figure 24 Ideal Current Sweep.

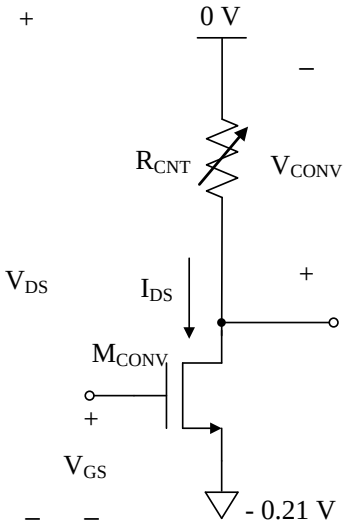

Figure 25 Ideal Resistance Sweep.

Two models are used in the performance evaluation of I-to-V conversion, a current-based DC sweep in Figure 24 and a resistance-based DC sweep in Figure 25.

The voltage from V_{DD} to V_{SS} is maintained at 0.21 V, to allow an approximate 0.2 V source-to-drain voltage across the CNT when configured in a voltage divider circuit shown in Figure 22 and Figure 23. Voltage sources of 0 and -0.21 V are used for the V_D and V_S terminals. The value of V_S can be adjusted by an external control to obtain data for other desired values of source to drain voltages across the CNT.

An ideal current source is used to test the I-to-V conversion circuitry with input currents of 0 to 100 nA. The purpose is to adjust the transistor width to length ratio for M_{CONV} that yields a resistance of around 1 MΩ to cover the potential current ranges of CNT. The value used for the control voltage V_{GS} is also another important design parameter to ensure the transistor stays in the linear region of operation. The results are shown in Figure 26 and Table 6. Since the value of V_{CONV} is a voltage value with respect to 0, a minor calculation is required to compute the voltage drop V_{CONV_M} across the transistor M_{CONV}.

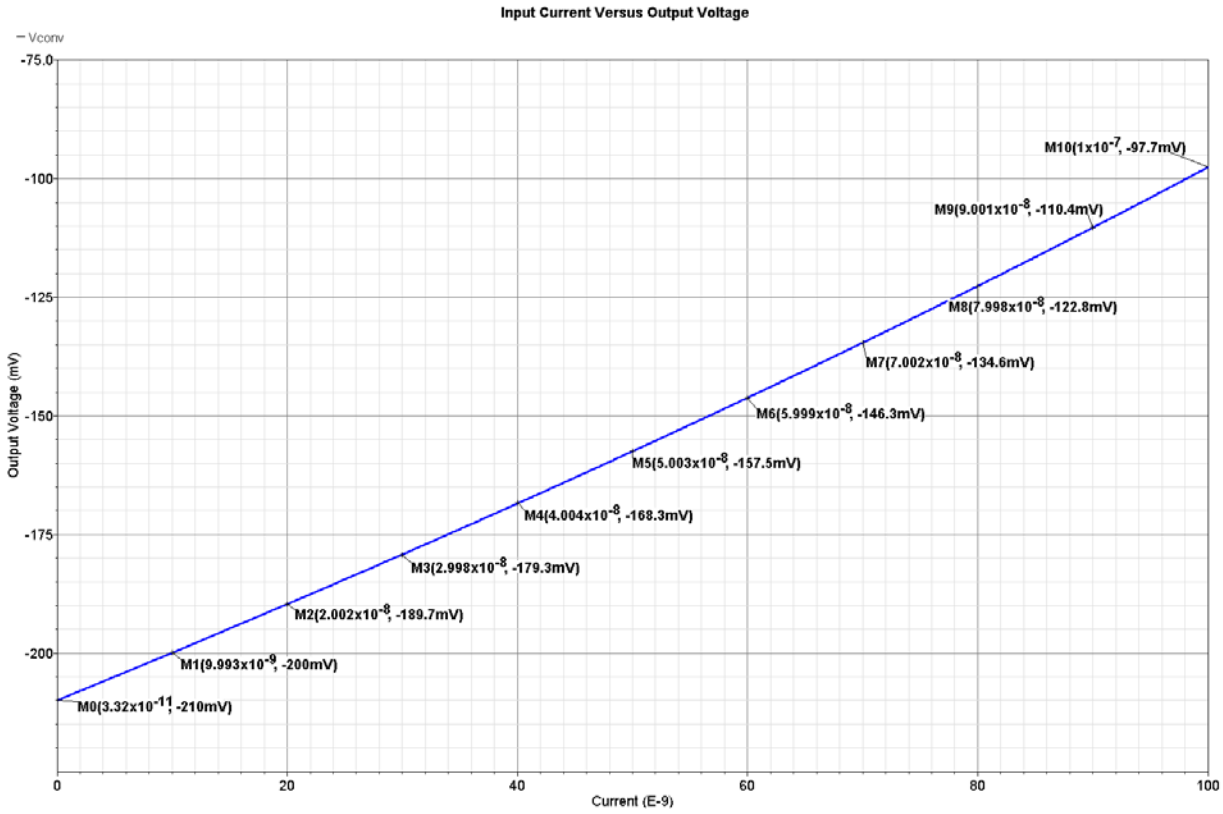

Figure 26 I-to-V Performance Evaluation with Input Current Sweep.

For a nominal value of 1MΩ, 1 nA of current will convert to approximately 1 mV. Thus it is crucial to preserve the linear relationship between the input current and the active transistor's ON-resistance. The table shows that for input currents of below 50 nA, the approximate conversion error is 5 %. The experimental value of 1.03 MΩ for R_{CONV} is used in subsequent analysis. It is noted that after fabrication, the variation of R_{CONV} can be calibrated to generate data similar to Table 6 and the calibrated results can be used for CNT analysis.

Table 8 I-to-V Performance Evaluation with Input Current.

Input Current (nA)	Vout (mV)	V_{CONV_M} (mV)	Estimated Resistance R_{CONV} (MΩ)
0	-210.0	000.0	0.000
10	-200.0	010.0	1.000
20	-189.7	020.3	1.015
30	-179.3	030.7	1.023
40	-168.3	041.7	1.043
50	-157.5	052.5	1.050
60	-146.3	063.7	1.062
70	-134.6	075.4	1.077
80	-122.8	087.2	1.090
90	-110.4	099.6	1.107
100	-097.7	112.3	1.123

An ideal resistor is used to test the I-to-V conversion circuitry, illustrated in Figure 25, ranging from 1 to 70 MΩ. The graph in Figure 27 shows the expected output voltage with respect to a given input resistance R_{CNT}.

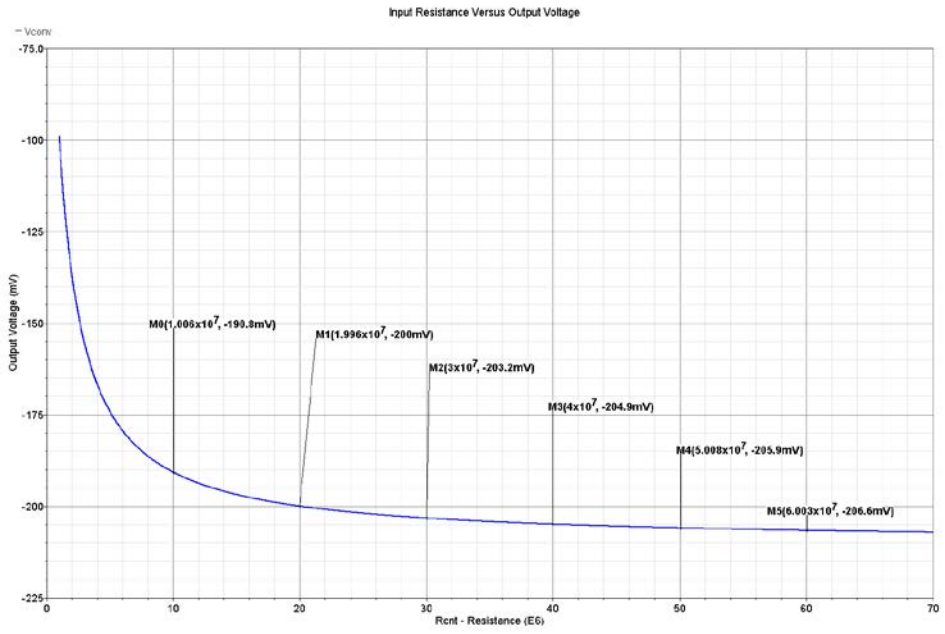

Figure 27 I-to-V Performance Evaluation with Input Resistance Sweep

Three sets of analysis data based on Figure 27 are presented in Table 7-9. Table 7 and 8 show the

relationship between the input resistance with the current and voltage drop across transistor M_{CONV}. Table 9 shows the estimated value of R_{CNT} based on the measured output voltage V_{CONV} and nominal R_{CONV} value of 1.03 MΩ. The ideal voltage drop across M_{CONV} is expressed in Equation 5.

$$V_{CONV\_M} = \frac{R_{CONV}}{R_{CNT} + R_{CONV}} * (V_D - V_S) \qquad \textbf{Equation 5}$$

The measured and ideal voltage drops across transistor M_{CONV} are V_{CONV_M} and V_{CONV_IDEAL} while the measured and ideal current through the same transistor are I_{CONV} and I_{CONV_IDEAL}. Table 7 shows a voltage error of less than 2 % while Table 8 shows a current error of less than 0.3 nA for the six data points in Figure 27. Table 9 shows an approximate 5 % error in the computed resistance of the senor device R_{CNT}. Again these errors can be essentially eliminated by making calibration measurements on the ROIC after fabrication.

Table 9 I-to-V Output Voltage Evaluation with Varying Input Resistance.

R_{CNT} (MΩ)	V_{CONV} (mV)	V_{CONV_M} (mV)	V_{CONV_IDEAL} (mV)	V Error (%)
10.06	-190.8	19.2	18.987	1.11
19.96	-200.0	10.0	10.019	0.19
30.00	-203.2	06.8	06.774	0.38
40.00	-204.9	05.1	05.122	0.43
50.08	-205.9	04.1	04.111	0.27
60.03	-206.6	03.4	03.441	1.21

Table 10 I-to-V Induced Current Evaluation with Varying Input Resistance.

R_{CNT} (MΩ)	V_{CONV_M} (mV)	I_{CONV} (nA)	I_{CONV_IDEAL} (nA)	Current Error (nA)
10.06	19.2	18.641	18.936	0.296
19.96	10.0	09.709	10.005	0.296
30.00	06.8	06.602	06.768	0.166
40.00	05.1	04.951	05.118	0.167
50.08	04.1	03.981	04.109	0.128
60.03	03.4	03.301	03.439	0.138

Table 11 I-to-V Estimated RCNT Value with Varying Input Resistance.

R_{CNT} (MΩ)	V_{CNT} (mV)	I_{CONV} (nA)	R_{CNT} (MΩ)	Resistance Error (%)
10.06	190.8	18.641	10.24	1.79
19.96	200.0	09.709	20.60	3.21
30.00	203.2	06.602	30.78	2.60
40.00	204.9	04.951	41.39	3.48
50.08	205.9	03.981	51.72	3.27
60.03	206.6	03.301	62.59	4.26

The final schematic design of the I-to-V convertor in Figure 23 used a very narrow and long transistor. The layout of the convertor is shown in Figure 28.

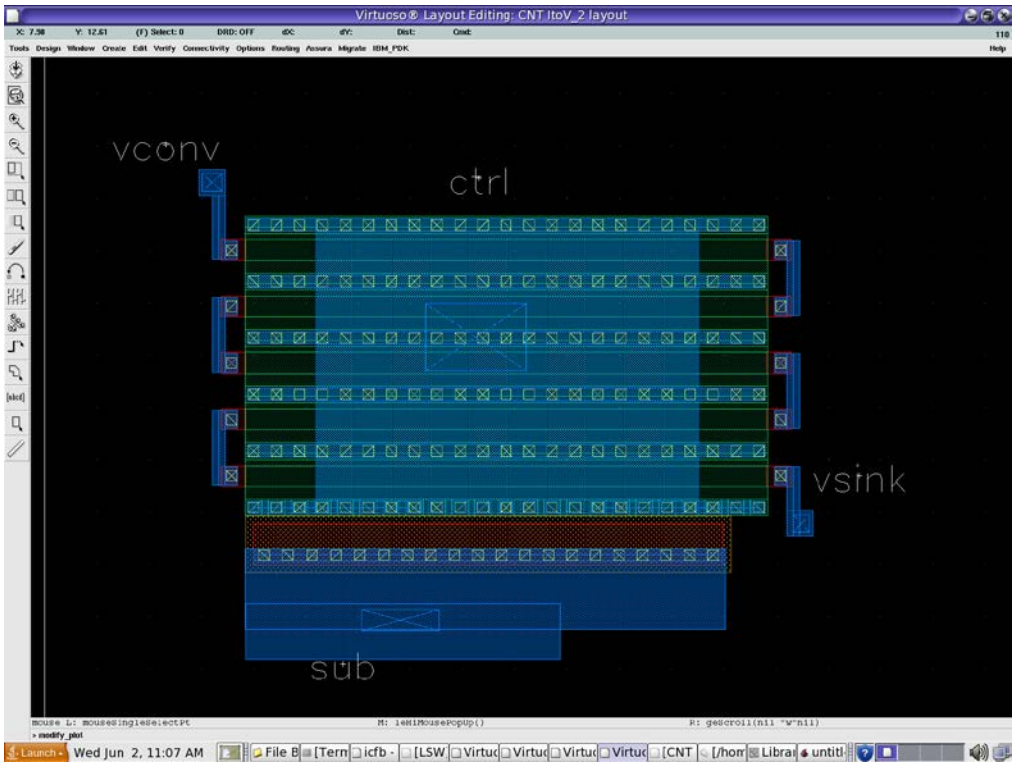

Figure 28 Layout Design of Current-to-Voltage Convertor.

9.5.2 Unity Gain Buffer and Voltage Amplification

The unity gain buffer and multi-stage gain are designed using different configurations of CMOS two-stage operational amplifiers (Op Amp), shown in Figure 29 and Figure 30.

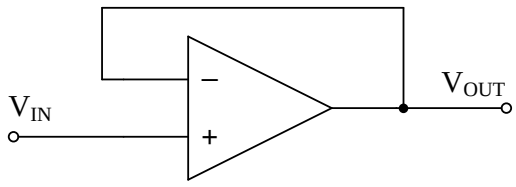

Figure 29 Unity Gain Buffer.

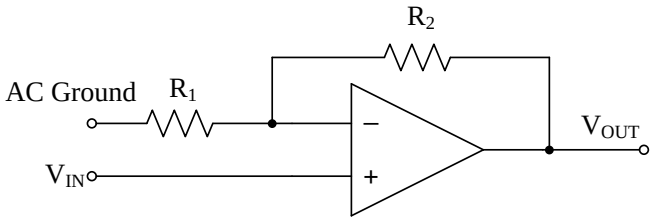

Figure 30 Non-Inverting Amplifier (1 Stage).

The transistor level diagram of the CMOS Op Amp is shown in Figure 31 and the layout in Figure 32. The labeled transistors and connections matches with the original transistor diagram of the operational amplifier in Figure 31.

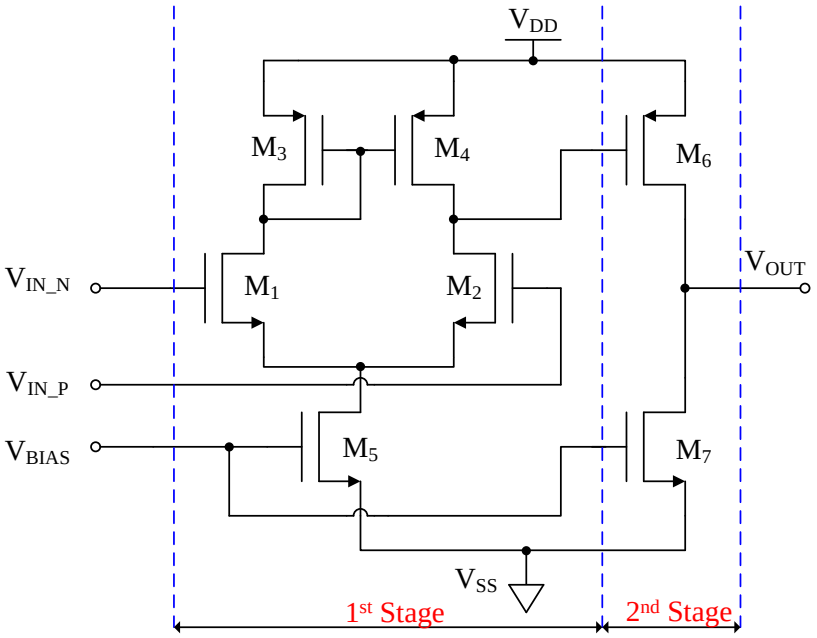

Figure 31 Two Stage CMOS Operational Amplifier Schematic Design.

The CMOS operational amplifier consists of an input differential stage with an output common-source amplifier stage. The first stage amplifies the difference in voltage between input ports V_{IN_P} and V_{IN_N} while the second stage provides bulk of the voltage gain needed. When used in the non-inverting amplifier configuration shown in Figure 20, the resistance values of R_1 and R_2 determines the gain of the amplifier. The multi-stage gain distribution stage of the TIA in Figure 20 uses numerous iterations of the inverting amplifier to reduce the resistance values needed to

maximize the voltage range from I-to-V conversion. This is essential in reducing the resistance values needed for a high gain to reduce the hardware overhead needed for fabricating on-chip resistors.

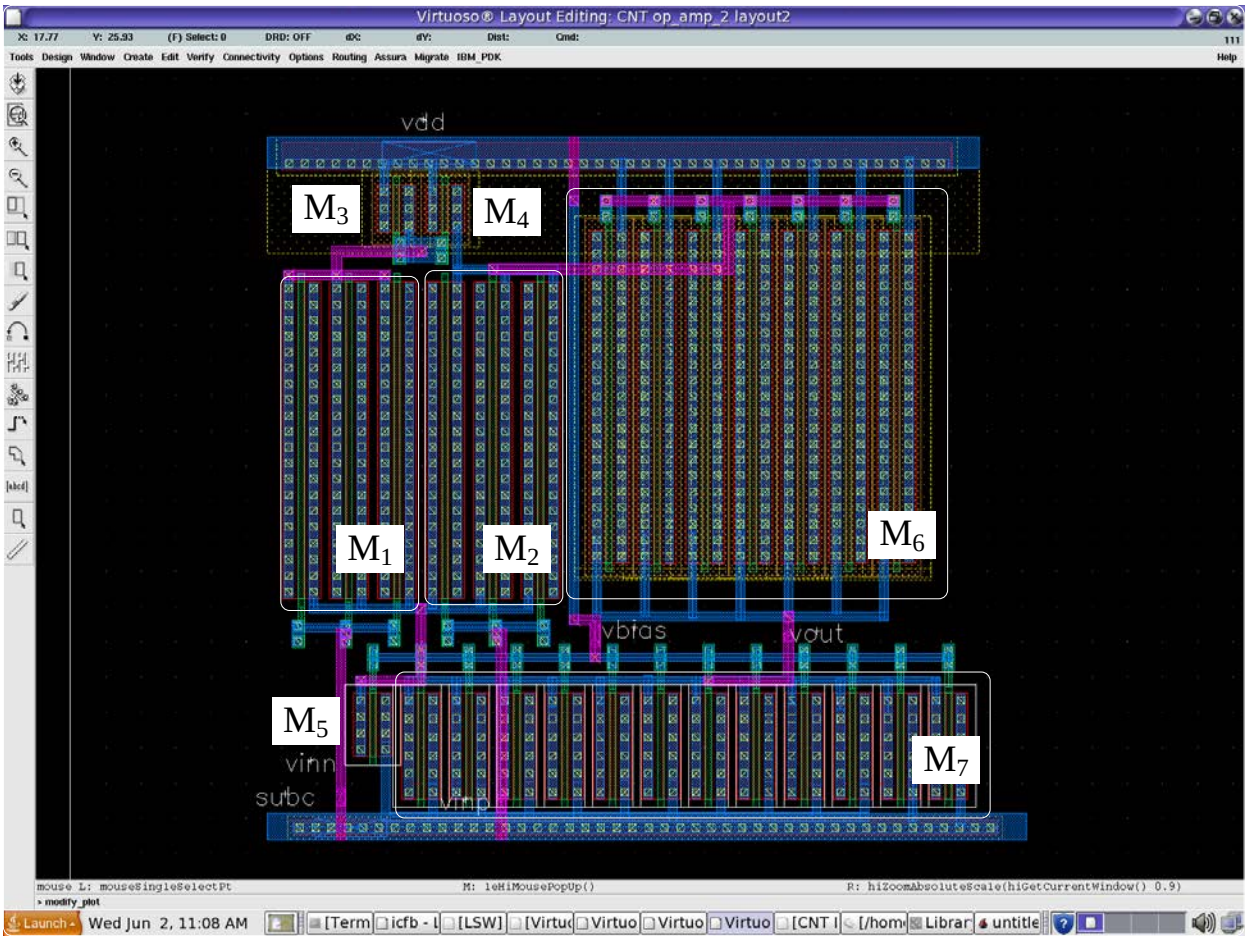

Figure 32 Two Stage CMOS Operational Amplifier Layout Design.

The following operations are performed using a seven transistor operational amplifier in various configurations. The non-inverting configuration amplifier, re-illustrated in Figure 33, is used extensively in the current TIA design.

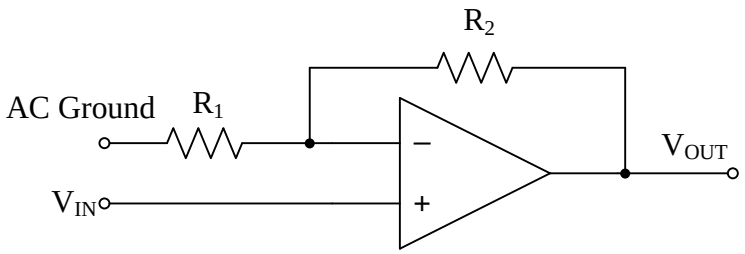

Figure 33 Non-Inverting Configuration.

Using the two golden rules of operational amplifiers with negative feedback, the input nodes have the same voltage values and that no current flows in or out of the input nodes, the gain of the non-inverting configuration can be calculated as follows,

$$\frac{V_{OUT}-V_{IN}}{R_2}=\frac{V_{IN}-V_{AC\_GND}}{R_1} \qquad \textbf{Equation 6}$$

$$R_1(V_{OUT}-V_{IN})=R_2(V_{IN}-V_{AC\_GND}) \qquad \textbf{Equation 7}$$

$$R_1V_{OUT}=V_{IN}(R_1+R_2)-R_2V_{AC\_GND} \qquad \textbf{Equation 8}$$

$$V_{OUT}=\left(1+\frac{R_2}{R_1}\right)V_{IN}-\frac{R_2}{R_1}V_{AC\_GND} \qquad \textbf{Equation 9}$$

When the AC ground is zero, the gain is approximately one plus the ratio of R_2 to R_1. The same circuit is used for DC shifting with identical resistances for R_1 and R_2. This yields the following equation with V_{AC_GND} is replaced with V_{ADJ} for the adjustment voltage required to shift the AC ground value to zero.

$$V_{OUT}=2V_{IN}-V_{ADJ} \qquad \textbf{Equation 10}$$

To shift the AC ground value or the center point of the detectable output voltage values from I-to-V to zero volts, the adjustment voltage is approximately two times the input offset voltage. This is required since the resulting converted voltage from I-to-V will be fairly close to the value of Vs in the TIA system shown in Figure 20. When amplified without DC shifting, the amplification will take place with Vs as the reference offset voltage, where some of the amplified values will be outside of the detectable range of the ADC. The range of acceptable input voltage value of the ADC is current set from 0.5 to -0.5 volts, thus it is crucial for the TIA to yield an amplified symmetric voltage waveform around zero volts. The subsequent voltage amplifiers

following DC shifting seeks to utilize the full range of the ADC with an approximate overall amplification of 32. The gain contribution of each TIA component is also shown in Figure 20.

The multi-stage gain amplification is presented in Figure 34, where three stages of operational amplifiers in non-inverting configuration is used. The approximate resistance ratios are presented with respect to R.

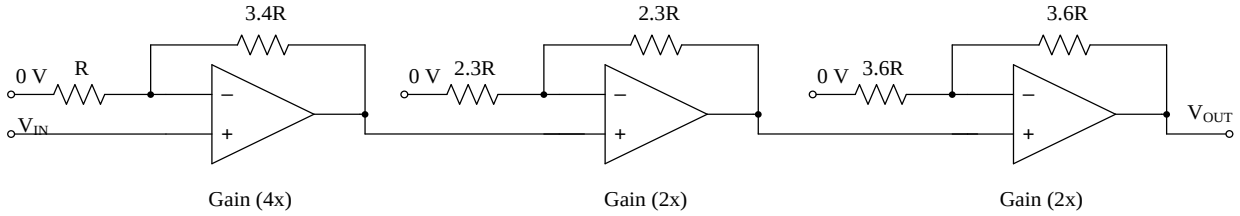

Figure 34 Multi-Stage Gain Distribution.

Multi-stage gain distribution is used to reduce the area consumption of the resistors with a series of lowered gain stages to minimize the resistance values required. The actual overall gain from DC shifting and multi-stage gain distribution is approximately 30.5 for the schematic design.

Figure 35 shows the core layout design of the CNT analysis system prior to the insertion of buffers, input/output pads for external chip connections, electro-static protection circuits, dummy components for chip density requirements, and analog-to-digital convertor for post digital signal processing algorithms.

The layouts of the above designs are extracted to find the connections between electrical devices, device parameter measurements, and parasitic devices with the associated measurements. Two main parameters are extracted along with the above components. The first parameter is the parasitic resistance extraction to calculate the distributed R and RC parasitics. And the second is the layout parasitics extraction to calculate the lumped C parasitic nets. The extracted TIA gain is 26.04.

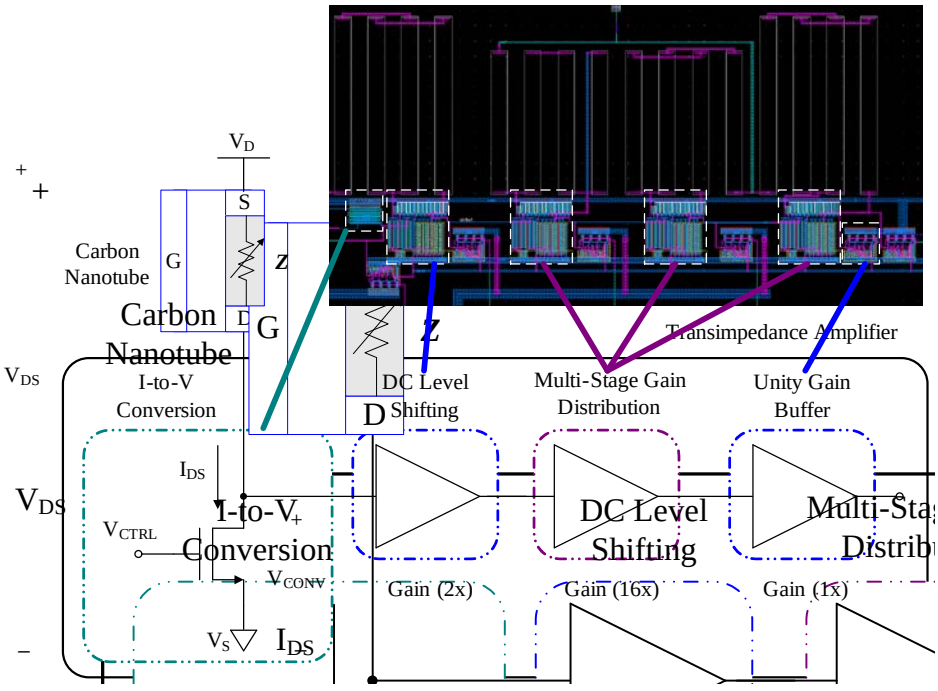

Figure 35 Trans-Impedance Amplifier Layout.

The blocks on top of DC level shifting and voltage amplifiers in Figure 35 are resistors.

Overall, the current architecture allows the Carbon nanotube sensor to experience an approximate source-to-drain voltage ranging from 0.21 to 0.41 volts. This is achieved by varying the value for V_S. Note that when changing Vs in Figure 20, the values for V_{CTRL} and V_{ADJ} will also need to be adjusted to maintain the resistance of M_{CONV} at 1 MΩ in addition to adjustments to DC shifting. Fortunately, the relationship between V_{CTRL} and V_{ADJ} to V_S is a first order linear equation and it can be easily implemented on the peripheral control board (PCB) with the use of voltage regulators as inputs to the readout integrated circuit (ROIC). This will enable the user to adjust only V_S while V_{CTRL} and V_{ADJ} are automatically adjusted.

9.5.3 Analog-to-Digital Conversion

Analog to digital conversion consists of the steps illustrated in Figure 36. The analog signal is first sampled, quantized to a digital format of ones and zeroes, and finally converted to an workable binary number format through the encoder. The digitized data can then be processed, modulated/demodulated, and transmitted through different signal and communication algorithms.

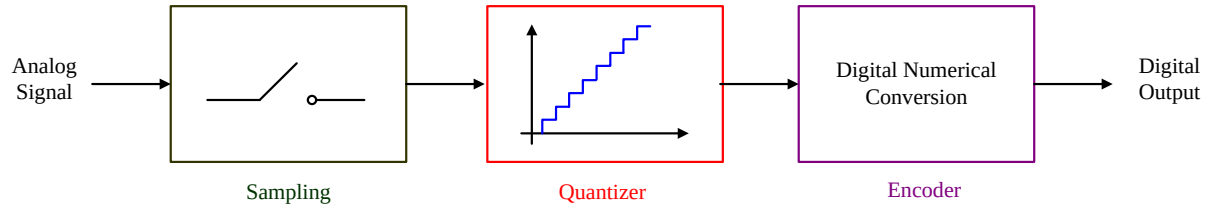

Figure 36 Analog to Digital Conversion.

The architecture used for our implementation is shown in Figure 37, for a flash-based 3-bit ADC for illustration purposes. For a N-bit flash ADC, it is composed of 2^N resistors, 2^N-1 comparators, and a 2^N-1 to N encoder. Thus for a 3-bit ADC, it requires 8 equal value resistors, 7 comparators, and a 7-to-1 encoder.

The series of equal value resistors forms a voltage divider, which creates seven reference voltages to sample the analog input with. Then the comparators are used to compare the input analog voltage value with the seven reference voltages at fixed time intervals. Zero indicates that the current voltage value is less than the reference voltage compared with and an one indicates the opposite. Generally, a clock with a fixed period and 50% duty cycle is used here for sampling at fixed time intervals. At the end of quantization, a 7-bit thermometer code composed of zeroes and ones are obtained, and then this is converted to a workable numerical format for post processing.

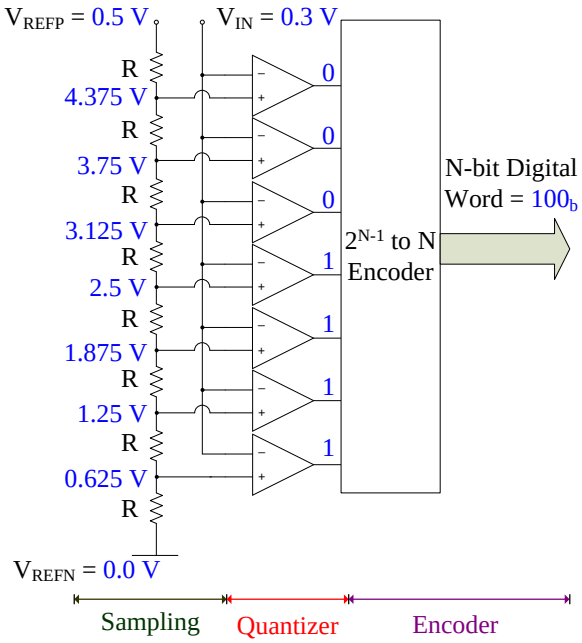

Figure 37 Flash-based Analog-to-Digital Convertor.

Table 12 is used to convert the 7-bit thermometer code to 3-bit binary number. The order of bits for thermometer code is from top-to-bottom, or from most to least significant bits, in Figure 37.

Table 12 Digital Output Codes.

Decimal	Thermometer	Binary
0	0000000	000
1	0000001	001
2	0000011	010
3	0000111	011
4	0001111	100
5	0011111	101
6	0111111	110
7	1111111	111

The above methodology is used to implement the 8-bit ADC. The transient analysis of the 8-bit ADC schematic design is shown in Figure 38. The clock pulse used has a period of 80 ns, thus the ADC samples at the falling edge of the clock pulse as indicated in the figure at every 80 ns.

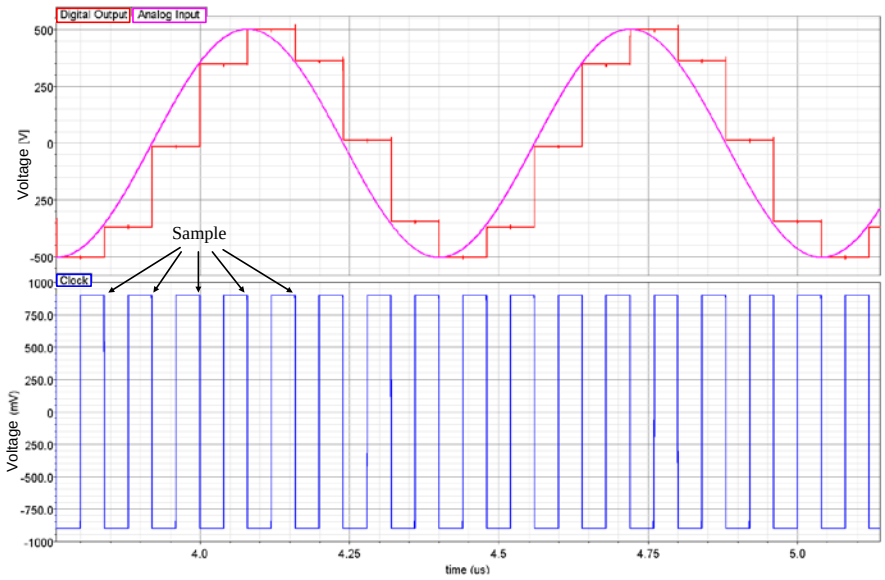

Figure 38 8-bit ADC Transient Analysis.

The digital output is normalized with respect to the original analog input amplitudes for comparison purposes. The above simulation result visually shows that the digital signal matches closely with the original analog input signal of 1.5625 MHz.

Spectral analysis using discrete Fourier transform is also used to evaluate the performance of the ADC. The FFT spectrum is shown in Figure 39.

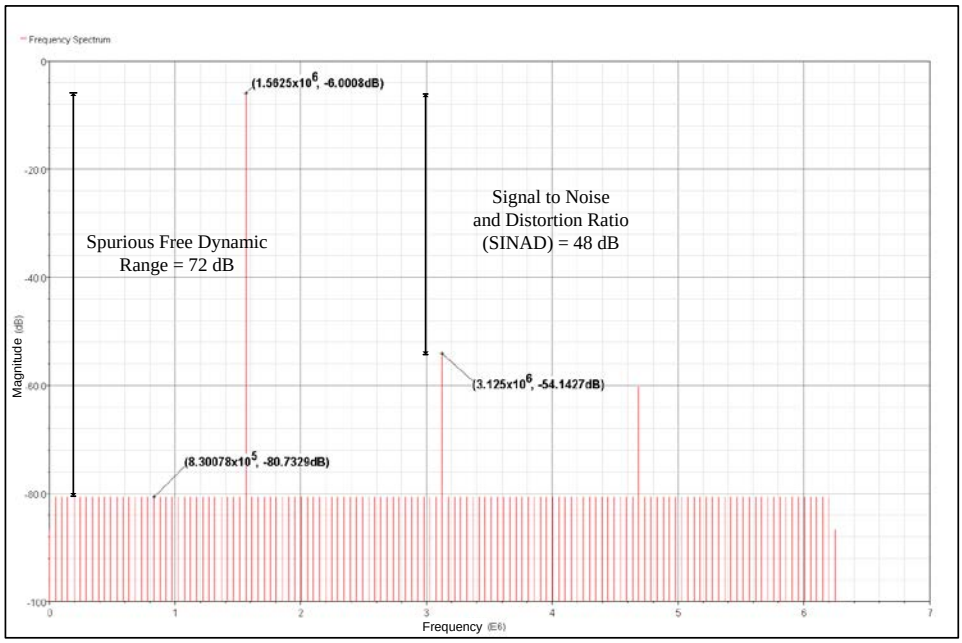

Figure 39 8-bit ADC Discrete Fourier Spectral Analysis.

Two methods are used in estimate the performance of the ADC from observing the spectrum of the digital output. Both involve measuring the power of the primary signal against other peaks in the spectrum. The primary magnitude measure the digitized signal amplitude strength at that frequency against others.

The first method measures the dB difference between the primary signal and the next highest spur, the signal to noise and distortion ratio (SINAD). The spurs in the frequency spectrum can be noise resulting from quantization or harmonics of the primary signal. SINAD is approximately equal to 6.02 times the effective number of bits (of the ADC). Thus taking the value from Figure 39, the ENOB is approximately 8.

The second method measures the dB difference between the primary signal and the next highest noise spur (excluding the harmonics of the primary signal), the spurious free dynamic range (SFDR). SFDR is approximately 9 times the effective number of bits (of the ADC). Thus taking the value from Figure 39, the ENOB is also approximately 8 in this case.

Both tests show that the ADC is able to utilize all 8-bits of the digital output; this is usually not the case in higher sampling ADC. The spectral tests are performed based on data points sampled at every 80 ns, which is significantly faster than the required sampling time of the CNT sensor.

Figure 40 is a snapshot of the 6-bit flash ADC designed. This is part of the 8-bit ADC planned for the project.

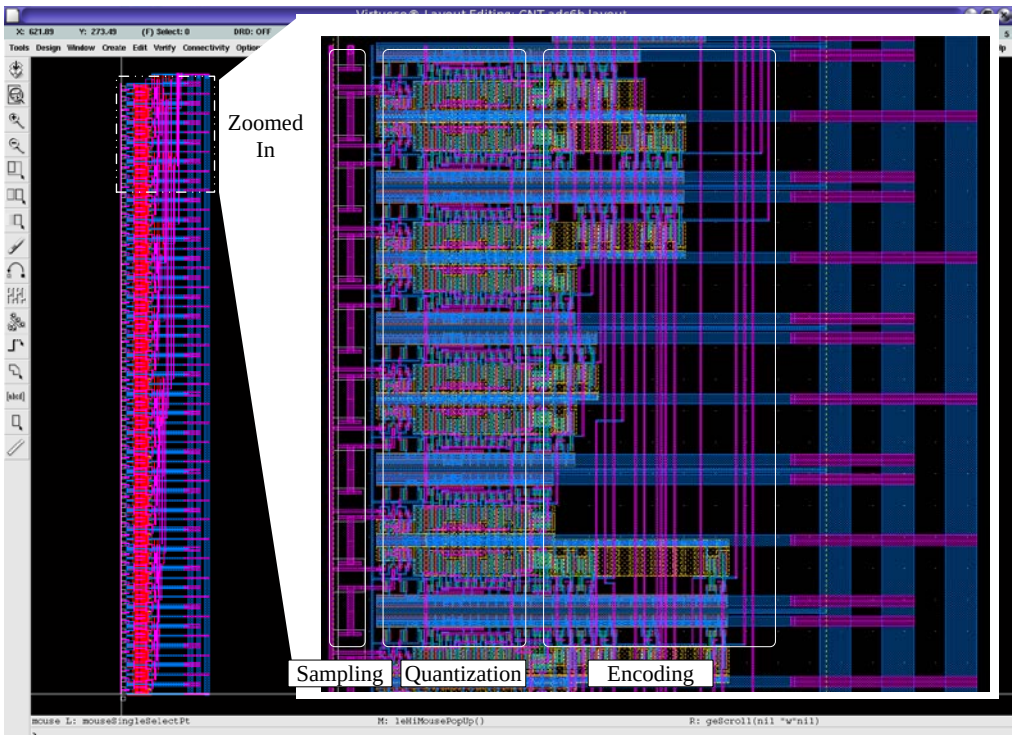

Figure 40 6-bit ADC Layout.

The snapshot shows the strings of CMOS resistors used for sampling, the comparator and related circuits for holding the digital values in quantization, and lastly, the digital logic gates and connections for encoding the thermometer code to a binary number.

9.5.4 Full Chip Layout and Dimensions for Final Fabrication

The original trans-impedance amplifier is shown in Figure 41 for reference. The full chip layout is shown in Figure 42. The major components of the readout integrated circuit include the primary trans-impedance amplifier, an 8-bit analog-to-digital convertor, and a secondary TIA for backup. This report shows the readout integrated circuit's carbon nanotube current estimation performance based on the I-to-V and TIA outputs. For the primary TIA, the V_S and V_{CTRL} nodes in Figure 41 are the input (I) pads for the chip in V_{SINK_1} and V_{CTRL_1} in Figure 42. Extra observation points after DC level shifting and within voltage amplification stages are also included. A secondary TIA is added in case the first fails, it only contains the I-to-V portion without the subsequent voltage amplification.

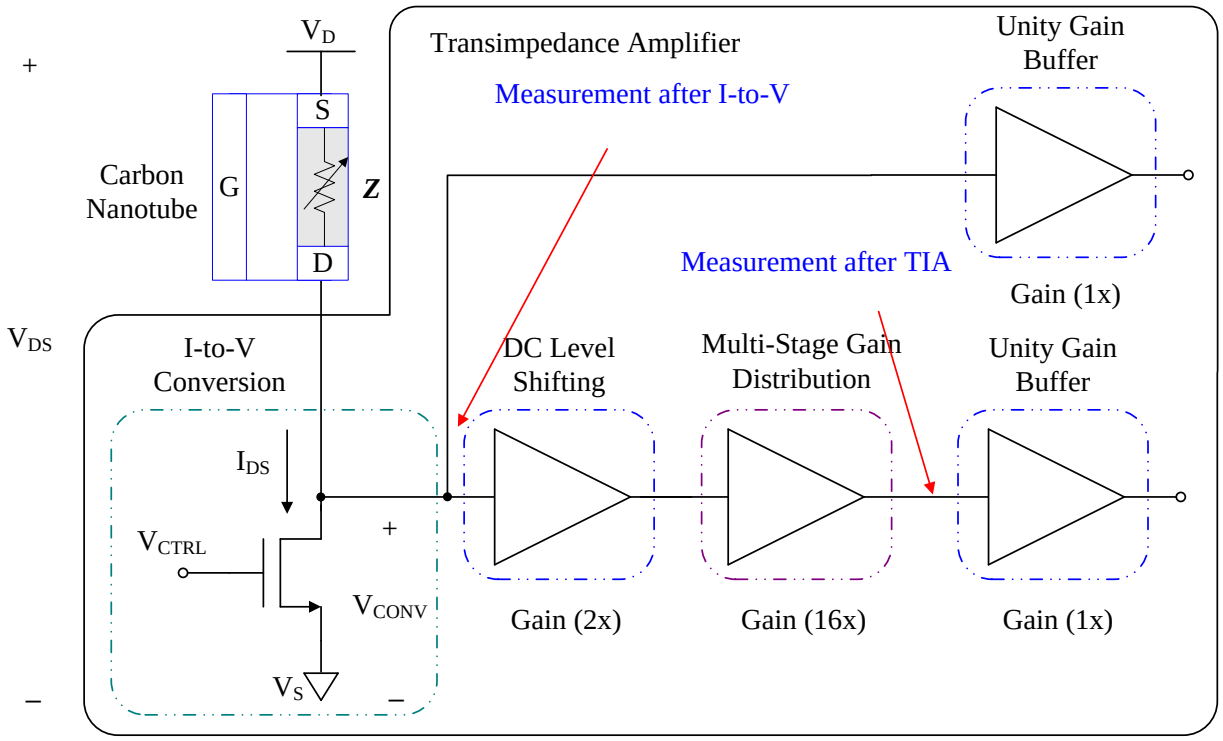

Figure 41 Trans-Impedance Amplifier Block Diagram.

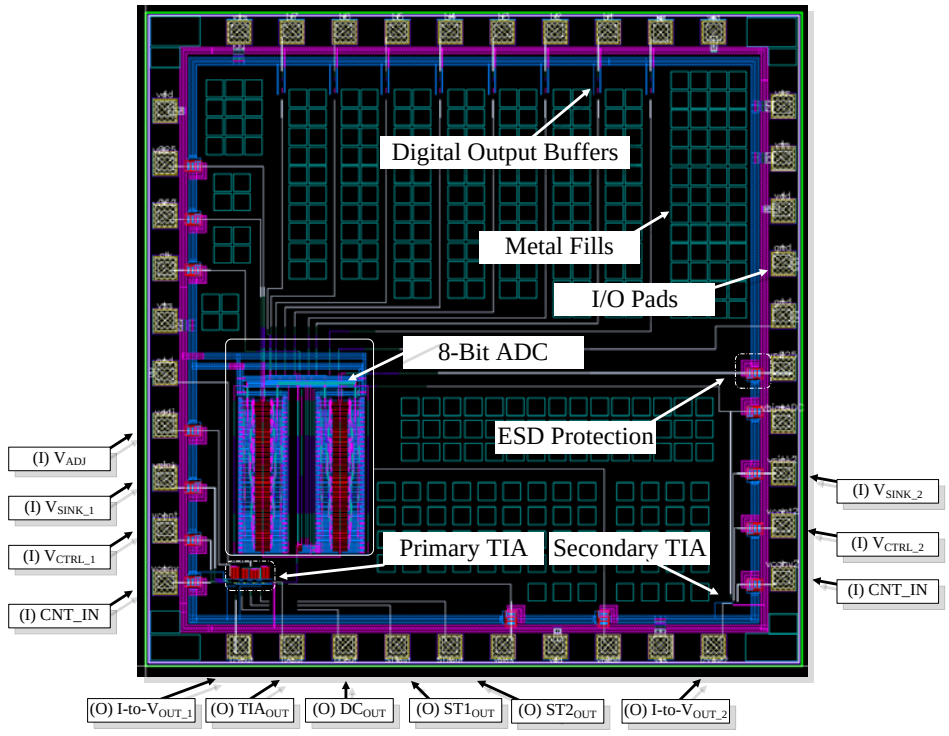

Figure 42 Full Chip Layout.

The dimensions of the major components in the readout integrated circuit are listed in Table 13. The width and length are the horizontal and vertical measurements of the components in Figure 42.

Table 13 Readout Integrated Circuit Component Dimensions.

Component	Width (um)	Length (um)
Full Chip	3039	3039
Primary TIA	199	107
Secondary TIA	30	30
8-bit ADC	617	936

9.5.5 Determination of Adjustable Parameters V_{CTRL} and V_{ADJ}

The maximum observed current of AFRL's fabricated CNT sensor is about 60 nA for source-to-drain voltage drop of less than 0.4 V. A current sweep using an ideal current source with various V_S, illustrated in Figure 43, is used to obtain the different control voltage V_{CTRL} to maintain the resistance of M_{CONV} at 1 MΩ.

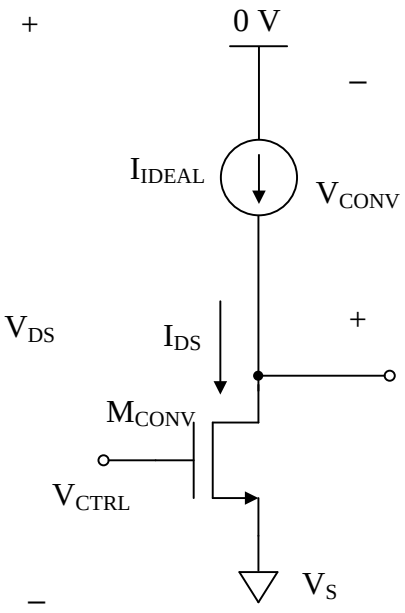

Figure 43 Ideal Current Sweep.

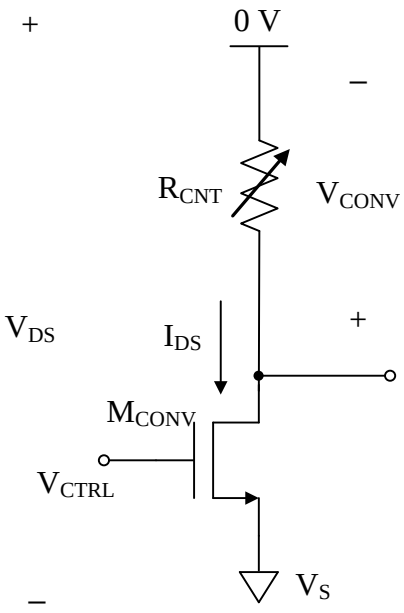

Figure 44 Ideal Resistance Sweep.

The control voltage is chosen such that when a 20 MΩ resistance is used for R_{CNT} in Figure 44,

R_{CONV} is equal to 1 MΩ. 20 MΩ is chosen based on the median value of AFRL's observed resistance values. A worst case 10% variation in resistance deviation is observed in the experimental data.

Table 14 lists the obtained control voltages to maintain a 1 MΩ resistance for I-to-V conversion. In addition, a source-to-drain current sweep is performed to estimate the expected resistance value of M_{CONV} based on the obtained control voltage.

Table 14 Control Voltage in I-to-V for Different Source-to-Drain Voltage across CNT.

V_S (V)	V_{CTRL} (V)	R_{CONV} (MΩ) for Each I_{DS}					
		10 nA	20 nA	30 nA	40 nA	50 nA	60 nA
-0.21	0.70395	1.011	1.036	1.062	1.091	1.122	1.155
-0.25	0.65913	1.008	1.033	1.059	1.087	1.118	1.151
-0.26	0.64681	1.010	1.035	1.061	1.089	1.120	1.154
-0.27	0.63457	1.012	1.036	1.063	1.091	1.122	1.156
-0.31	0.58980	1.009	1.033	1.059	1.087	1.118	1.152
-0.32	0.58122	1.003	1.026	1.052	1.080	1.110	1.143
-0.35	0.54484	1.006	1.030	1.056	1.084	1.114	1.148
-0.36	0.53591	1.000	1.024	1.050	1.077	1.107	1.140
-0.37	0.52381	1.001	1.025	1.051	1.078	1.108	1.141
-0.41	0.47846	0.999	1.023	1.048	1.076	1.105	1.138

The configuration in Figure 44 is then used to acquire the expected output voltage from I-to-V conversion. Since most of the resistance value falls between 10 and 70 MΩ in AFRL's existing device, this is the range of resistance values used for the sweep. The intent is to find the median value of the output voltage and use this as a guide to obtain the adjustment voltage required for DC shifting. The attained adjustment voltages are listed in Table 15. Vpp is the peak-to-peak voltage range after I-to-V conversion with respect to the resistance sweep. Vmid is the median value used to find the DC adjustment required. For example, for Vs of -0.31 V, the expected output voltage after I-to-V conversion is -0.2935 V ± 12.2 mV. Note that the table is a reduced set of data obtained from the simulation.

Table 15 Adjustment Voltage for DC Shifting.

V_S (V)	I-to-V Voltage (V) with R_{CNT} Sweep				Vpp (mV)	Vmid (V)	V_{ADJ} (V)
	10 MΩ	30 MΩ	50 MΩ	70 MΩ			
-0.21	-0.1907	-0.2033	-0.2059	-0.2071	16.4	-0.1989	-0.4072
-0.25	-0.2270	-0.2420	-0.2452	-0.4265	19.5	-0.2368	-0.4847
-0.26	-0.2360	-0.2516	-0.2549	-0.2564	20.3	-0.2462	-0.5040
-0.27	-0.2451	-0.2613	-0.2647	-0.2662	21.1	-0.2557	-0.5234
-0.31	-0.2813	-0.3000	-0.3040	-0.3057	24.4	-0.2935	-0.6008
-0.32	-0.2905	-0.3098	-0.3138	-0.3156	25.1	-0.3031	-0.6205
-0.35	-0.3176	-0.3388	-0.3432	-0.3451	27.5	-0.3314	-0.6787
-0.36	-0.3268	-0.3485	-0.3530	-0.3550	28.2	-0.3409	-0.6983
-0.37	-0.3358	-0.3582	-0.3928	-0.3649	29.1	-0.3504	-0.7180
-0.41	-0.3720	-0.3969	-0.4021	-0.4043	32.3	-0.3882	-0.7968

9.5.6 ROIC Schematic and Layout Simulation and Performance Evaluation

Based on the feedback from midterm review in early April and consultation with Dr. Sang Nyon Kim in late May, minor improvements were made on the preliminary schematic design to improve the source-to-drain current estimation in the CNT analysis system. This chapter provides the nodal voltage and current measurement results for both the final schematic design and layout design for final fabrication.

This chapter shows the voltage outputs after current-to-voltage (I-to-V) conversion and trans-impedance amplifier (TIA) indicated in the top level schematic diagram in Figure 45. Although not shown in the diagram, but output ports are inserted between each of the functional components within the TIA for observation in the final fabricated CMOS chip. Measured data for these nodes are available but not included in this report.

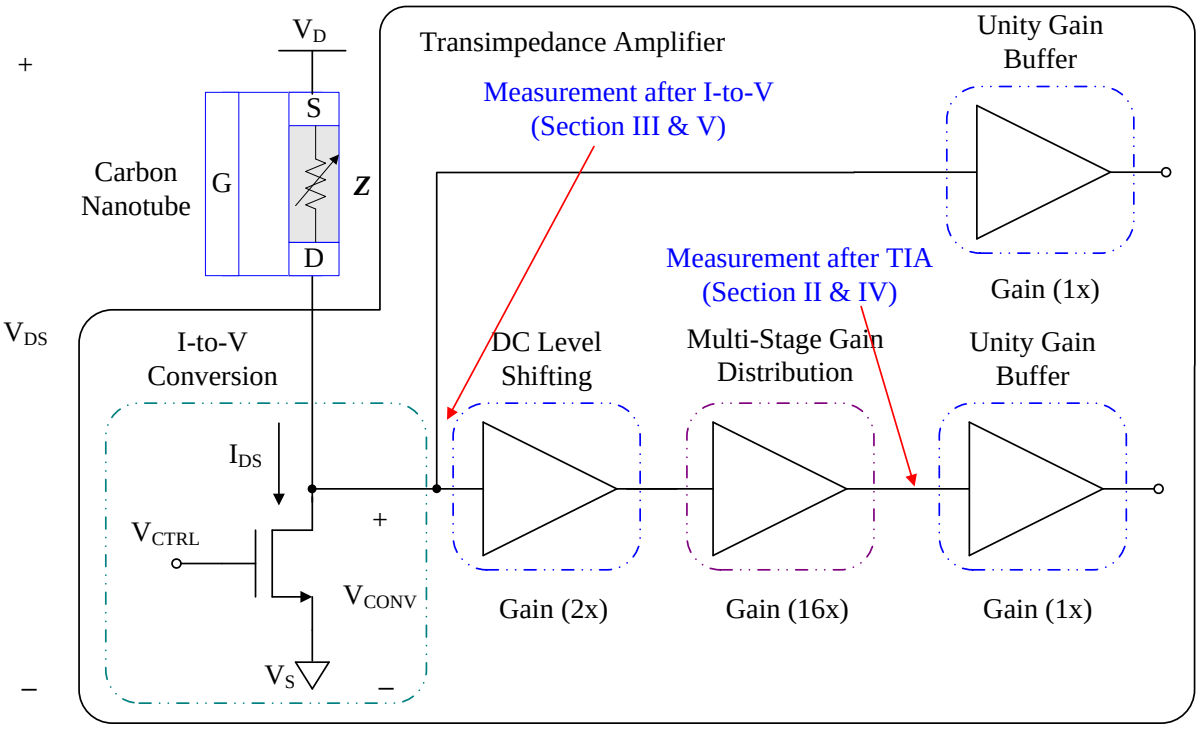

Figure 45 Trans-Impedance Amplifier (TIA).

The color conventions of the data used are as follows, **blue** is AFRL's reference data, **red** and **green** are the estimated source-to-drain current/voltage values based on output voltage of a given node, and **black** is the measured voltage value at that node. The **red** data is for the schematic design while the **green** is for the layout design.

Sections 9.5.6.1 and 9.5.6.2 present the current estimation based on the outputs in the **schematic** designs of TIA and I-to-V conversion. Sections 9.5.6.3 and 9.5.6.4 present the current estimation based on the outputs in the **layout** designs of TIA and I-to-V conversion. Section 9.5.6.5 compares the estimated source-to-drain current through the CNT sensor for **schematic** and **layout** based designs.

9.5.6.1 Current Estimation Based on Trans-Impedance Amplifier Output (Schematic)

The following results are based on Dr. Kim's original captured data recorded on the excel sheet. Based on the original source-to-drain current and voltage values, the resistance across the device can be computed and the expected source-to-drain current flow across the sensor when put in series with the current-to-voltage (I-to-V) convertor can be approximated. Table 16 lists the reference current used at the drain terminal of the I-to-V convertor in nano amperes.

Table 16 Expected Source-to-Drain Current Across Sensor (AFRL Reference) [nA].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	21.4871	20.6917	19.2575	17.8825	14.9956	8.6218
-0.31	31.7354	30.5019	28.4307	26.4777	22.0543	12.9768
-0.41	41.9993	40.3136	37.6433	35.0434	29.3153	16.9029

Based on the respective source-to-drain voltages applied across the sensor and convertor connected in series, the measured output voltage of the TIA is tabulated in Table 17.

Table 17 Measured TIA Output Voltage [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	306.494	282.77	240.059	199.300	114.104	-71.755
-0.31	460.039	422.393	359.389	300.246	167.281	-100.819
-0.41	615.023	562.799	480.330	400.484	226.211	-142.843

Using the information in Table 17 and knowing the precise voltage shifted during the DC Level Shifting block of -0.1989, -0.2935, and -0.3882 V for source-to-drain voltages of 0.21, 0.31, and 0.41 volts, the estimated current across the sensor is approximated in Table 18, Table 19, and Table 20.

Table 18 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.21 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	21.4871	21.5784	0.0913	0.42
-10	20.6917	20.7588	0.0671	0.32
-5	19.2575	19.2833	0.0258	0.13
0	17.8825	17.8752	0.0073	0.04
5	14.9956	14.9320	0.0636	0.42
10	8.6218	8.5112	0.1106	1.28

Table 19 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.31 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	31.7354	31.9134	0.1780	0.56
-10	30.5019	30.6255	0.1236	0.41
-5	28.4307	28.4703	0.0396	0.14
0	26.4777	26.4472	0.0305	0.12
5	22.0543	21.8988	0.1555	0.71
10	12.9768	12.7277	0.2491	1.92

Table 20 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.41 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	41.9993	41.9993	0.0000	0.00
-10	40.3136	40.2302	0.0834	0.21
-5	37.6433	37.4365	0.2068	0.55
0	35.0434	34.7317	0.3117	0.89
5	29.3153	28.8281	0.4872	1.66
10	16.9029	16.3262	0.5767	3.41

For the estimated source-to-drain current in the original design specification, where the source-to-drain voltage is set at 0.21 volts, the estimated error is less than **1.28 %**. When taking into account the estimated error for the three different source-to-drain voltage used, the maximum estimated error is at **3.41 %**.

The above tabulated data may be better expressed in terms of their graphical representation in Figure 46, where the reference AFRL data is in **blue** and the estimated source-to-drain current based on the output of TIA is in **red**. The same coloring convention is used in the tabulated data as well.

The estimated current error for the source-to-drain current estimation could be better with further fine tuning in the control voltage used for the I-to-V converter if the approximate CNT source-to-drain current value range for each gate voltage is known.

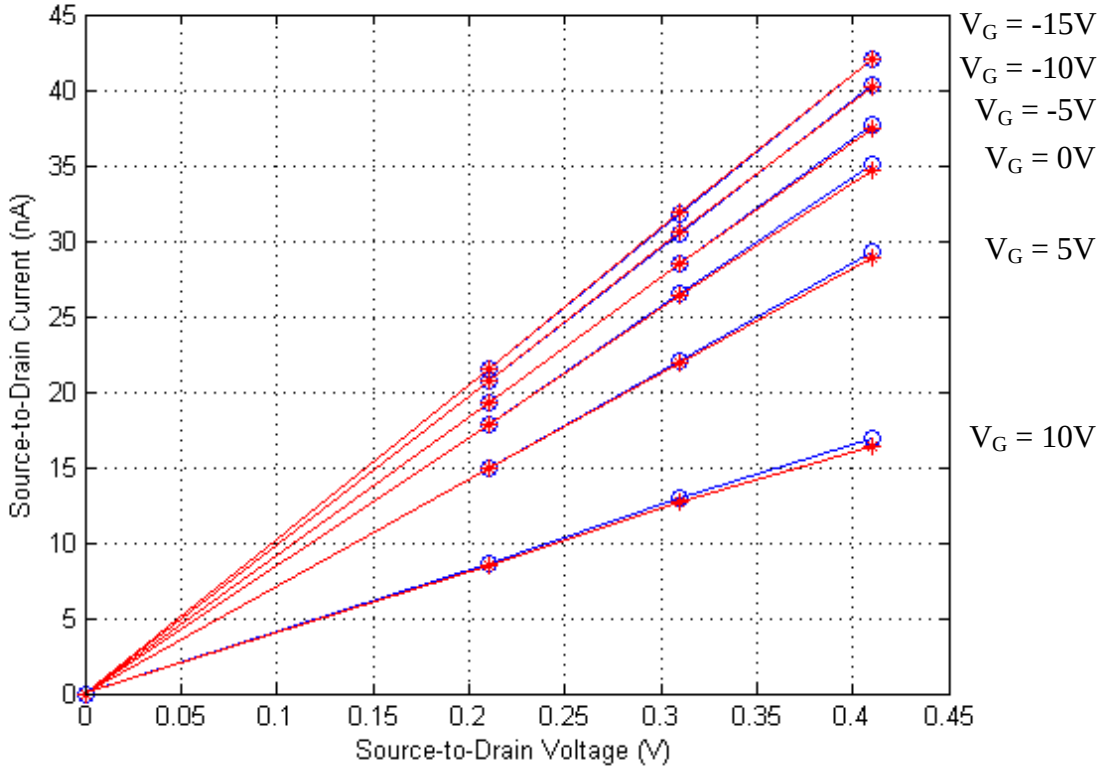

Figure 46 Estimated and Reference Source-to-Drain Current Comparison.

The original tuning for the control voltage was based on the old data that approximated the range of current values will be contained within 0 to 30 nA. However, the resistance of the I-to-V convertor will vary about 1-2% for input current values that are 10 nA away from the original reference current point used for fine tuning. Thus if a different control voltage is used for each change in the gate voltage of the CNT sensor, the estimated current data will be much better. Another important note is that this fine tuning can be performed at any point of the chip design cycle, from schematic, layout, to the final fabricated device.

For comparison purposes in later discussions, the estimated voltage at the output of I-to-V convertor (based on knowing the TIA output voltage) without direct measurement at that node is tabulated in Table 21.

Table 21 Estimated Voltage Following I-TO-V Convertor Based on TIA Output [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	-188.206	-189.034	-190.524	-191.946	-194.919	-201.404
-0.31	-277.448	-278.762	-280.960	-283.024	-287.663	-297.018
-0.41	-366.741	-368.563	-371.440	-374.226	-380.307	-393.184

9.5.6.2 Current Estimation Based on I-to-V Conversion Output (Schematic)

In the schematic circuit simulation, the output voltage following **I-to-V conversion** is tabulated in Table 22. The same AFRL data set is used for these simulations.

Table 22 Measured Output Voltage Following I-TO-V Conversion [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	-188.218	-189.044	-190.531	-191.950	-194.916	-201.392
-0.31	-277.517	-278.827	-281.018	-283.074	-287.693	-297.015
-0.41	-366.883	-368.702	-371.568	-374.339	-380.377	-393.171

In comparison with Table 21, for source-to-drain voltage of 0.21 volts, the error between the actual and estimated voltage at the output node of I-TO-V conversion is approximately 0.01 mV. The worst case voltage estimation error is when the source-to-drain voltage used is 0.41 volts, where the errors are about 0.15 mV, or 0.04 %.

The source-to-drain current across the sensor could also be estimated using similar equations used for the output of the TIA. The estimated current flow through the sensor for source-to-drain voltages of 0.21, 0.31, and 0.41 volts are recorded in TABLES 6.2.2, 6.2.3, and 6.2.4.

Comparing Table 23 to Table 18, Table 24 to Table 19, and Table 25 to Table 20, in sections 9.5.6.1 and 9.5.6.2, they show similar error percentages in the estimated current flow. This indicates that the use of DC level shifting and voltage amplifiers did not have a significant effect on the source-to-drain estimation.

Table 23 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.21 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	21.4871	21.5663	0.0792	0.37
-10	20.6917	20.7485	0.0568	0.27
-5	19.2575	19.2762	0.0187	0.10
0	17.8825	17.8713	0.0112	0.06
5	14.9956	14.9347	0.0609	0.41
10	8.6218	8.5228	0.0990	1.15

Table 24 Comparison of Estimated Source-to-Drain Current Across Sensor (Vs = -0.31 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	31.7354	31.8461	0.1107	0.35
-10	30.5019	30.5618	0.0599	0.20
-5	28.4307	28.4137	0.0170	0.06
0	26.4777	26.3980	0.0797	0.30
5	22.0543	21.8696	0.1847	0.84
10	12.9768	12.7304	0.2464	1.90

Table 25 Comparison of Estimated Source-to-Drain Current Across Sensor (Vs = -0.41 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	41.9993	41.8612	0.1381	0.33
-10	40.3136	40.0951	0.2185	0.54
-5	37.6433	37.3126	0.3307	0.88
0	35.0434	34.6223	0.4211	1.20
5	29.3153	28.7602	0.5551	1.89
10	16.9029	16.3388	0.5641	3.34

V_{CTRL} plays a critical role in controlling the resistance of the I-to-V conversion which will impact the final estimation sensor current result. Prior to plugging in the CNT sensor, the value

of V_{CTRL} must be tuned according to a controlled resistance value for a fixed source-to-drain voltage across the location where the CNT sensor will be located.

Similar to the analysis in section 9.5.6.1, the results in Table 23, Table 24, and Table 25 can be shown graphically as depicted in Figure 47. Comparison between Figure 46 and Figure 47 shows no observable change in the estimated current flow through the CNT sensor.

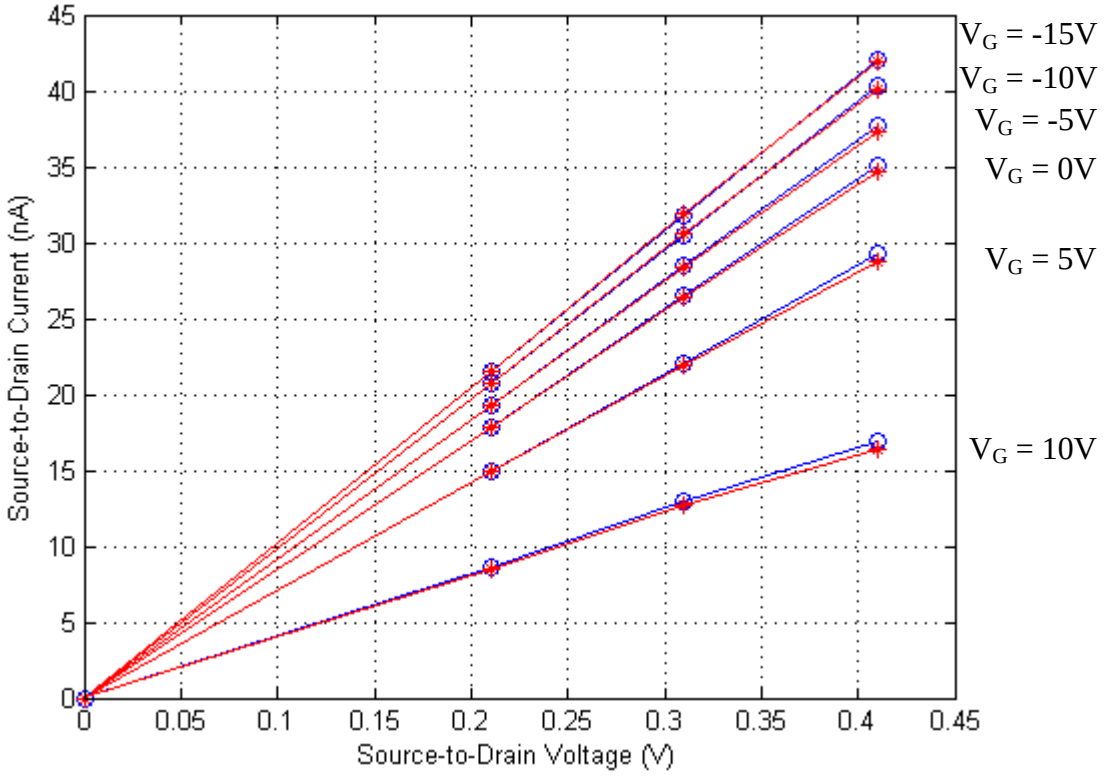

Figure 47 Estimated and Reference Source-to-Drain Current Comparison.

9.5.6.3 Current Estimation Based on Trans-Impedance Amplifier Output (Layout)

The reference data used in the layout simulation is the same as the one used for the schematic based transistor design and re-tabulated in Table 26.

Table 26 Expected Source-to-Drain Current across Sensor (AFRL Reference) [nA].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	21.4871	20.6917	19.2575	17.8825	14.9956	8.6218
-0.31	31.7354	30.5019	28.4307	26.4777	22.0543	12.9768
-0.41	41.9993	40.3136	37.6433	35.0434	29.3153	16.9029

Based on the respective source-to-drain voltages applied across the sensor in Table 26 and I-to-V convertor connected in series, the measured output voltage of the TIA is tabulated in Table 27.

Table 27 Measured TIA Output Voltage [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	279.655	258.092	219.279	182.247	104.869	-63.723
-0.31	417.973	383.741	326.461	272.702	151.896	-91.283
-0.41	558.472	510.921	435.866	363.220	204.74032	-130.143

Using the information in Table 27 and knowing the precise voltage shifted during the DC Level Shifting block of -0.1989, -0.2935, and -0.3882 V for source-to-drain voltages of 0.21, 0.31, and 0.41 volts, the estimated current across the sensor is approximated in Table 28, Table 29, and Table 30.

Table 28 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.21 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	21.4871	21.6296	0.1426	0.66
-10	20.6917	20.8098	0.1178	0.57
-5	19.2575	19.3340	0.0770	0.40
0	17.8825	17.9260	0.0430	0.24
5	14.9956	14.9839	0.0121	0.08
10	8.6218	8.5734	0.0486	0.56

Table 29 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.31 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	31.7354	31.9218	0.1868	0.59
-10	30.5019	30.6329	0.1309	0.43
-5	28.4307	28.4764	0.0454	0.16
0	26.4777	26.4524	0.0256	0.10
5	22.0543	21.9041	0.1499	0.68
10	12.9768	12.7485	0.2285	1.76

For the estimated source-to-drain current following the original design specification, where the source-to-drain voltage is set at 0.21 volts, the estimated error is less than **0.66 %**, better than the **1.28 %** reported for the schematic design.

Table 30 Comparison of Estimated Source-to-Drain Current Across Sensor (Vs = -0.41 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]	
-15	41.9993	42.0284	0.0294	0.07	
-10	40.3136	40.2555	0.0585	0.15	
-5	37.6433	37.4571	0.1859	0.49	
0	35.0434	34.7486	0.2944	0.84	
5	29.3153	28.8398	0.4752	1.62	
10	16.9029	16.3541	0.5489	3.25	

When taking into account the estimated error for the three different source-to-drain voltage used, the maximum estimated error is at **3.25 %**, matching the performance of the schematic circuit design.

Similar to section 9.5.6.1, the above tabulated data may be expressed in Figure 48, where the reference AFRL data is in **blue** and the estimated source-to-drain current based on the output of TIA is in **green**.

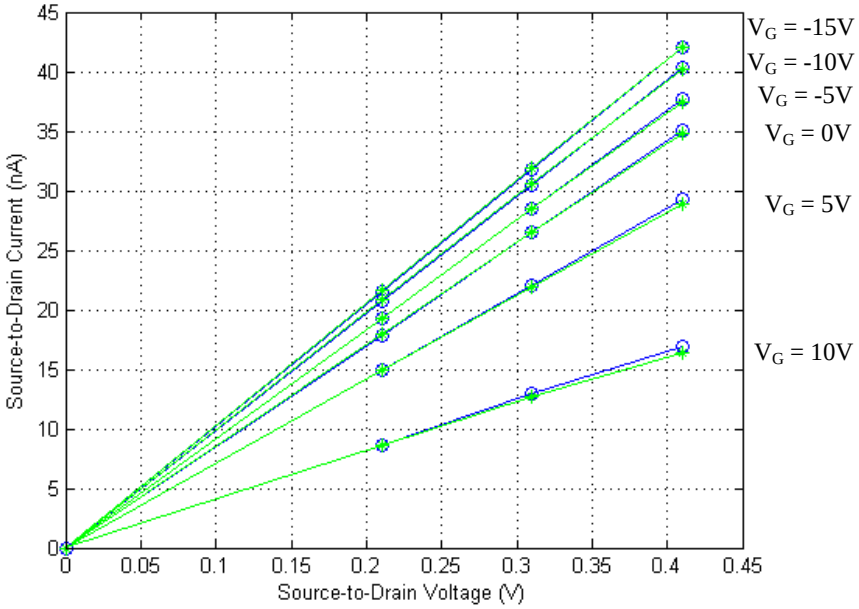

Figure 48 Estimated and Reference Source-to-Drain Current Comparison.

Note that although the gain through the entire TIA may be different from the original schematic design, but the resulting current estimation is still fairly similar to the original simulation data. The estimated voltage at the output of I-to-V convertor (based on knowing the TIA output voltage) without direct measurement at that node is tabulated in Table 31.

Table 31 Estimated Output Voltage After I-to-V Conversion Based on TIA Output [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	-188.161	-188.989	-190.479	-191.901	-194.873	-201.347
-0.31	-277.449	-278.763	-280.963	-283.028	-287.667	-297.006
-0.41	-366.753	-368.579	-371.461	-374.251	-380.337	-393.198

9.5.6.4 Current Estimation Based on I-to-V Conversion Output (Layout)

In the schematic circuit simulation, the output voltage following I-to-V conversion is tabulated in Table 32. The same AFRL data set is used for these simulations.

Table 32 Measured Output Voltage Following I-to-V Conversion [mV].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	-188.234	-189.059	-190.544	-191.961	-194.924	-201.397
-0.31	-277.553	-278.861	-281.048	-283.100	-287.712	-297.024
-0.41	-366.929	-368.744	-371.605	-374.370	-380.400	-393.179

In comparison with Table 31, for source-to-drain voltage of 0.21 volts, the error between the actual and estimated voltage at the output node of I-to-V conversion is approximately 0.07 mV. The worst case voltage estimation error is when the source-to-drain voltage used is 0.41 volts, where the errors are about 0.17 mV, or 0.05 %.

The source-to-drain current across the sensor could also be estimated using similar equations used in section 9.3. The estimated current flow through the sensor for source-to-drain voltages of 0.21, 0.31, and 0.41 volts are recorded in Table 33, Table 34, and Table 35.

Table 33 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.21 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	21.4871	21.5505	0.0635	0.30
-10	20.6917	20.7337	0.0417	0.20
-5	19.2575	19.2634	0.0064	0.03
0	17.8825	17.8604	0.0226	0.13
5	14.9956	14.9267	0.0693	0.46
10	8.6218	8.5178	0.1042	1.21

Table 34 Comparison of Estimated Source-to-Drain Current across Sensor (Vs = -0.31 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	31.7354	31.8108	0.0758	0.24
-10	30.5019	30.5284	0.0264	0.09
-5	28.4307	28.3843	0.0467	0.16
0	26.4777	26.3725	0.1055	0.40
5	22.0543	21.8510	0.2030	0.92
10	12.9768	12.7216	0.2554	1.97

Table 35 Comparison of Estimated Source-to-Drain Current Across Sensor (Vs = -0.41 V).

V_{GATE} [V]	I_{CNT} - AFRL [nA]	I_{CNT} - TIA [nA]	I_{CNT} - Error [nA]	I_{CNT} - Error [%]
-15	41.9993	41.8165	0.1825	0.43
-10	40.3136	40.0544	0.2596	0.64
-5	37.6433	37.2767	0.3663	0.97
0	35.0434	34.5922	0.4508	1.29
5	29.3153	28.7379	0.5771	1.97
10	16.9029	16.3311	0.5719	3.38

Comparing Table 33 to Table 28, Table 34 to Table 29, and Table 35 to Table 30, in sections 9.5.6.3 and 9.5.6.4, they show similar error percentages in the estimated current flow.

The main factor in controlling the estimated sensor current result is mostly based on how well the resistance of the I-to-V convertor is controlled via V_{CTRL}. For a fixed source-to-drain voltage across the CNT sensor, once the range of current for each varying gate voltage is identified, V_{CTRL} can be further fine-tuned to change with each gate voltage instead of remaining a fixed voltage source throughout the operation.

Similar to the analysis in the section 9.5.6.2, the results in Table 33, Table 34, and Table 35 can be shown graphically as depicted in Figure 49. Comparison between Figure 48 and Figure 49 shows no observable change in the estimated current flow through the CNT sensor.

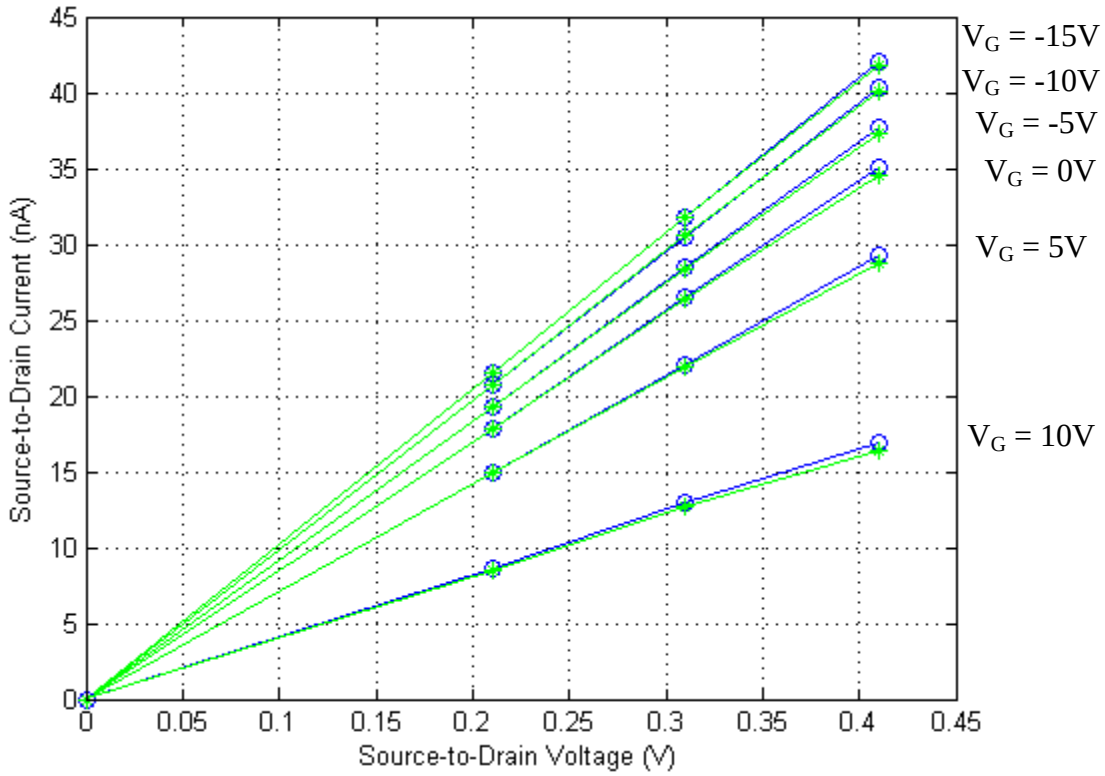

Figure 49 Estimated and Reference Source-to-Drain Current Comparison.

The above results are based on the spice simulation of the extracted layout with parasitic resistance and capacitances.

9.5.6.5 Estimated Current Comparison between Schematic and Layout

The estimated source-to-drain current based on the TIA output is used for comparison between the **schematic** and **layout** performance against AFRL's **reference** data. The results are plotted in Figure 50.

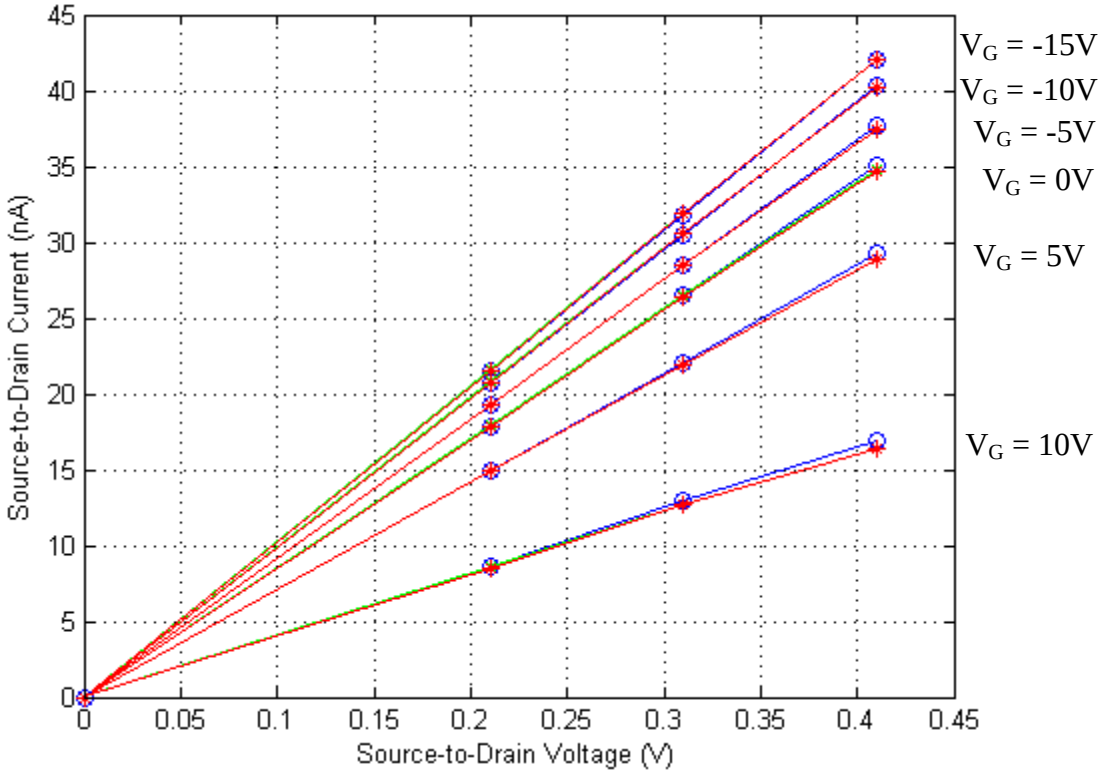

Figure 50 Schematic, Layout, and Reference Source-to-Drain Current Estimation Comparison.

Although not significantly visible, but the estimation of the source-to-drain current across the CNT of the extract layout design with associated parasitics matches well with the schematic based design. This is possible due to the flexibility of the V_{CTRL} and V_{ADJ} ports to fine tune the resistance value of the I-to-V convertor and aligning the DC level for subsequent voltage amplification within the TIA.

9.5.7 PCB Board Design to Interface CNT Sensor with ROIC

The final peripheral component board (PCB) design to interface the CNT sensor and the read-out integrated circuit is discussed in this chapter. The final system block diagram for the phase I prototype is shown in Figure 51.

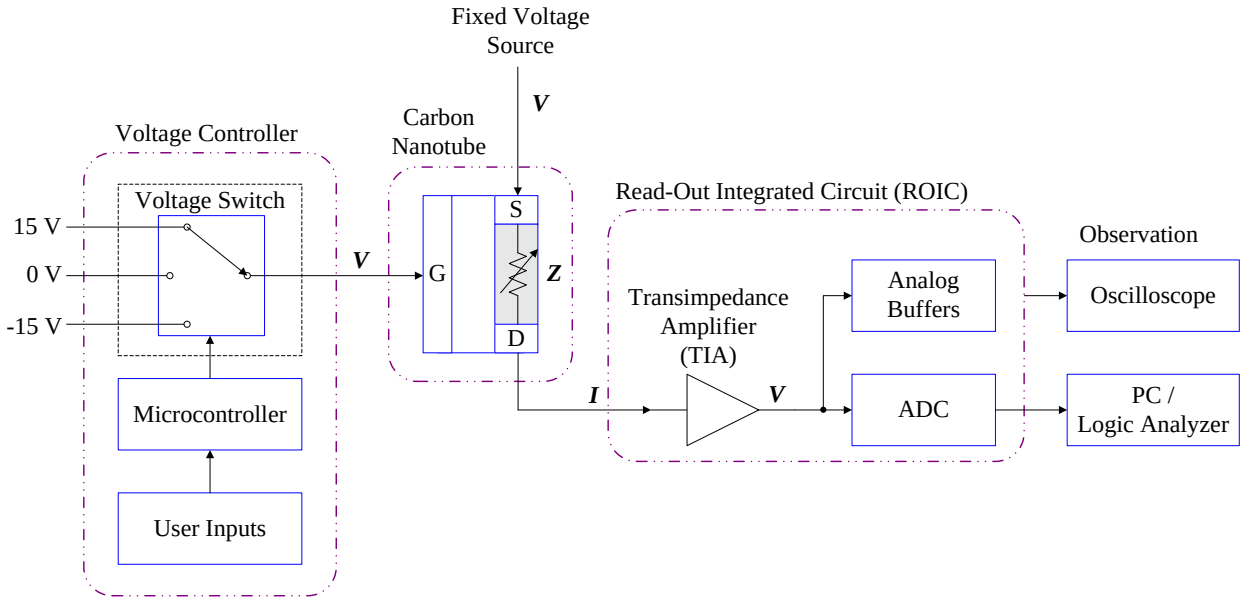

Figure 51 Phase I CNT Analysis System Block Diagram.

The tunable parameters V_{CTRL} and V_{ADJ} adjust the I-to-V conversion linearity and voltage amplification of the TIA to maximize the efficient use of the ADC.

The design specification of the voltage controller is illustrated in Figure 52, where the gate voltage is cycled automatically from a fixed positive voltage, to ground, and to fixed negative voltage

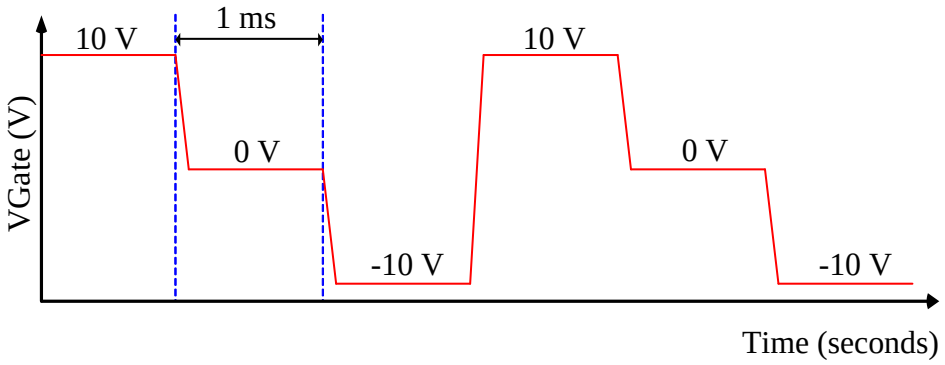

Figure 52 Voltage Controller Design Requirements.

Figure 51, the nanotube sensor, the read-out integrated circuit, and the voltage controller is interfaced with the PCB board design shown in Figure 53. The nanotube sensor is soldered to a disposable and removable sensor tray. Currently, four sensors may be placed in the tray for testing.

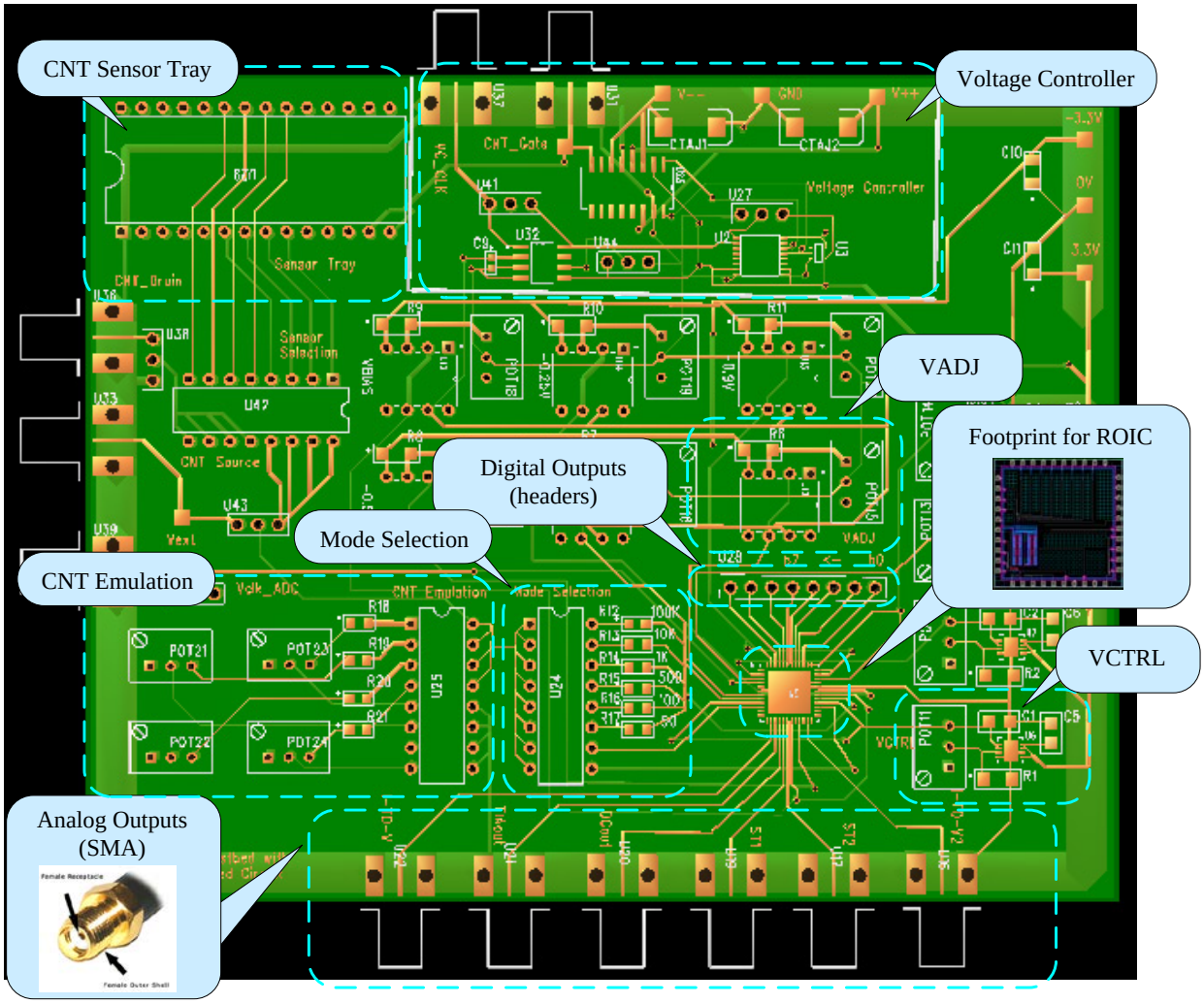

Figure 53 Completed PCB Design.

The location of the two adjustable parameters VCTRL and VADJ are placed sufficiently close to the read-out integrated circuit footprint (ROIC). The analog and digital port connections for observing the TIA outputs using oscilloscope and digital logic analyzer are also shown in Figure 53.

The voltage controller design following the specification in Figure 52 is shown in Figure 54. The voltage switch is an analog 4-to-1 multiplexor and is connected to the positive voltage (V++), GND, and negative voltage (V--) potentials. The fixed voltage inputs may have a range of ±4.5V to ± 20V. The microcontroller is a simple mod-2 counter design composed of a counter IC (U2) and inverter IC (U3), where the user may reset the controller using the dip switch in U27.

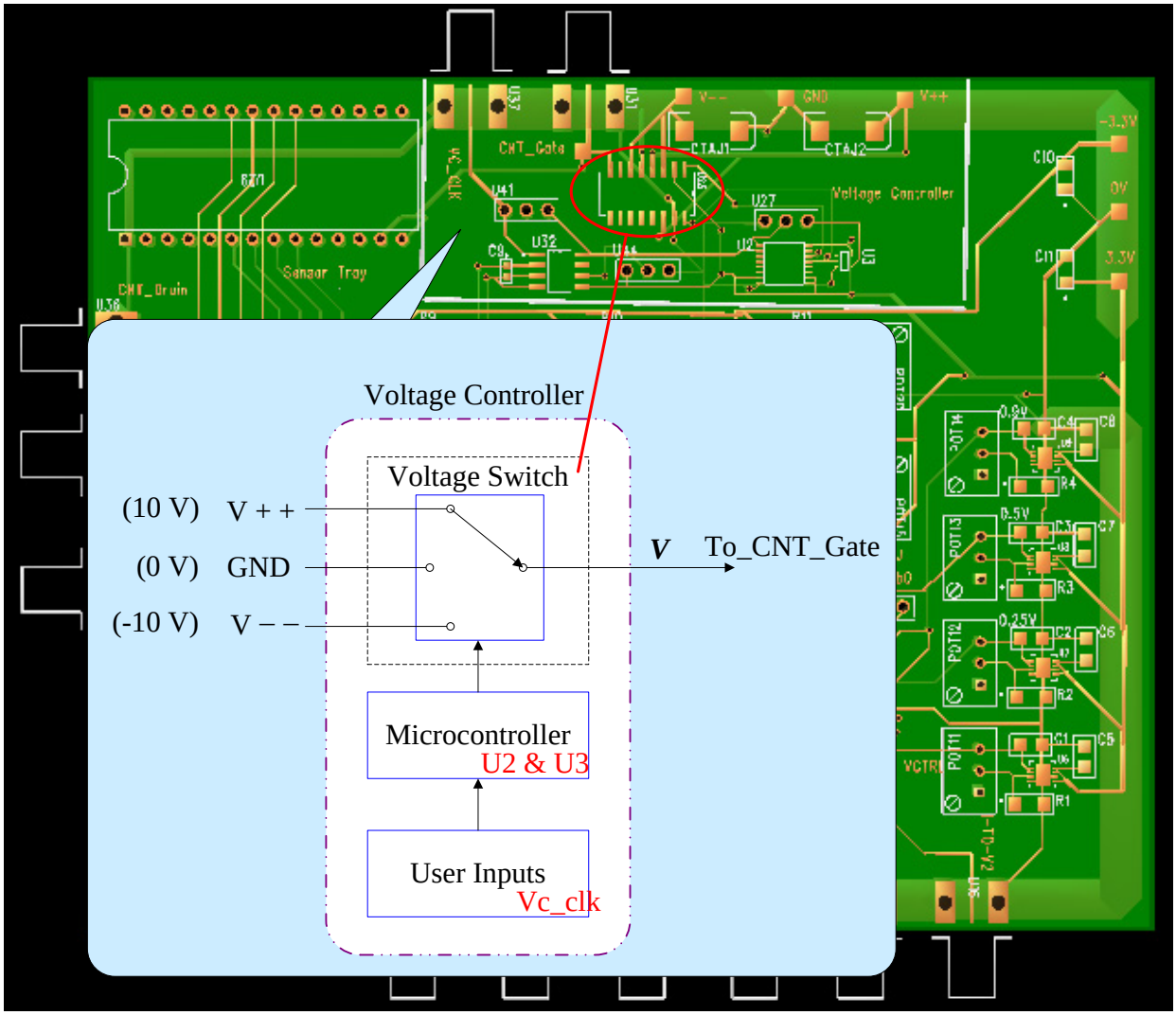

Figure 54 Voltage Controller Module Location.

The user inputs the intended cycle/pulsing period using an external waveform generator. The range of possible output frequency is from 1 mHz to greater than 5 MHz, which corresponds to the pulsing period from 0.2 µs to 16.67 minutes.

For emulating the behavior of the CNT sensor prior to sensor connection, the PCB board contains adjustable resistors to facilitate the testing. The resistance values of the emulated sensor are presented in Chapter 8.3 and re-tabulated in Table 36. Four possible combinations of sensor profiles are available for testing individually and the circuitry shown in Figure 55.

Table 36 Effective Sensor Resistance across Source-to-Drain (AFRL Reference) [MΩ].

V_S [V]	Gate Voltage [V]					
	-15	-10	-5	0	5	10
-0.21	9.308	9.666	10.386	11.184	13.337	23.197
-0.31	9.453	9.835	10.552	11.330	13.603	23.118
-0.41	9.524	9.922	10.626	11.414	13.645	23.665

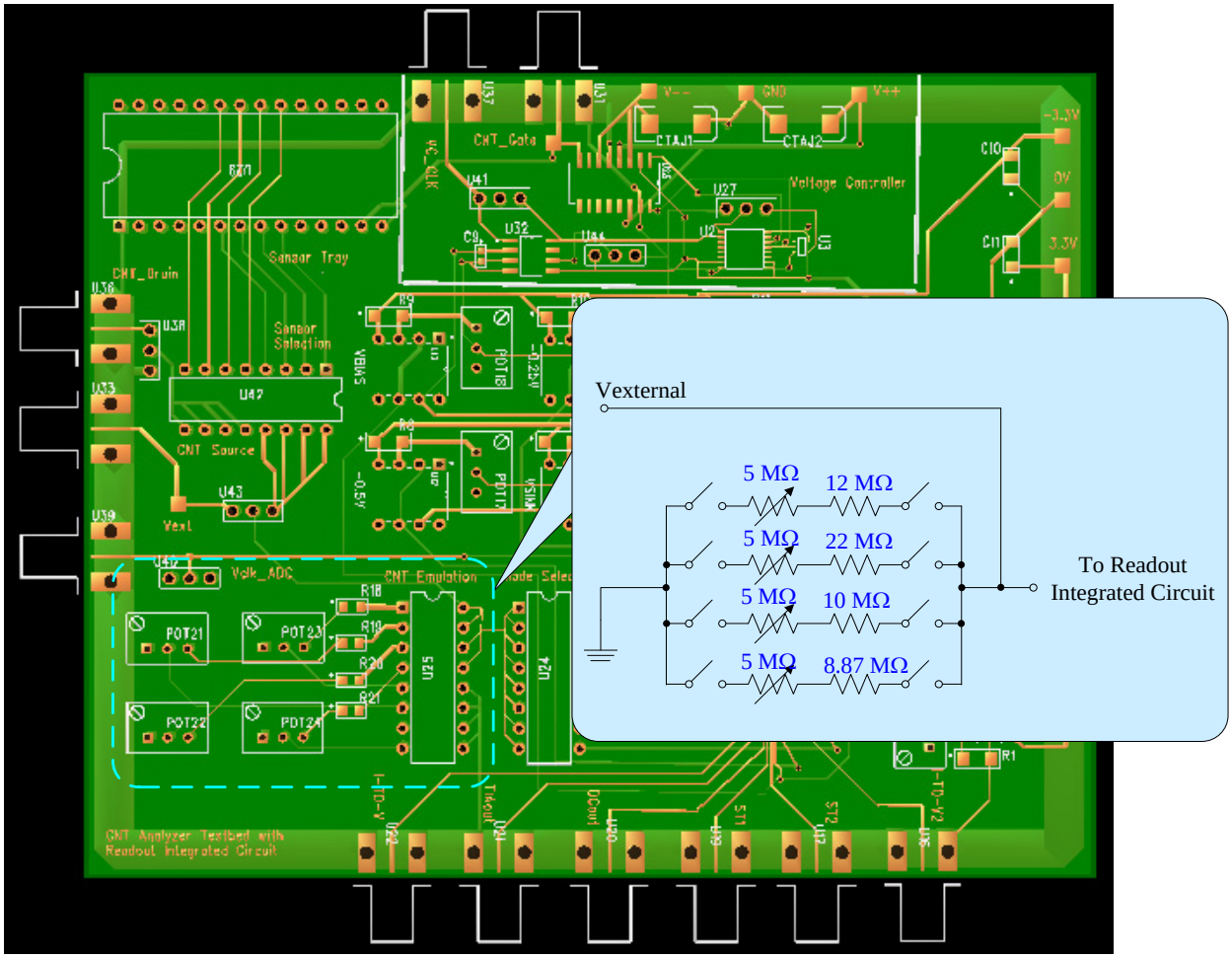

Figure 55 CNT Emulation Circuitry.

In addition to the originally planned sensor profiles, addition high precision resistors (0.05% error) are placed on the board with control dip switches in parallel with the I-to-V convertor on

the TIA in ROIC. The block diagram of the design for expanded usage is shown in Figure 56 and the ranges of the estimated detectable current ranges are tabulated in Table 37.

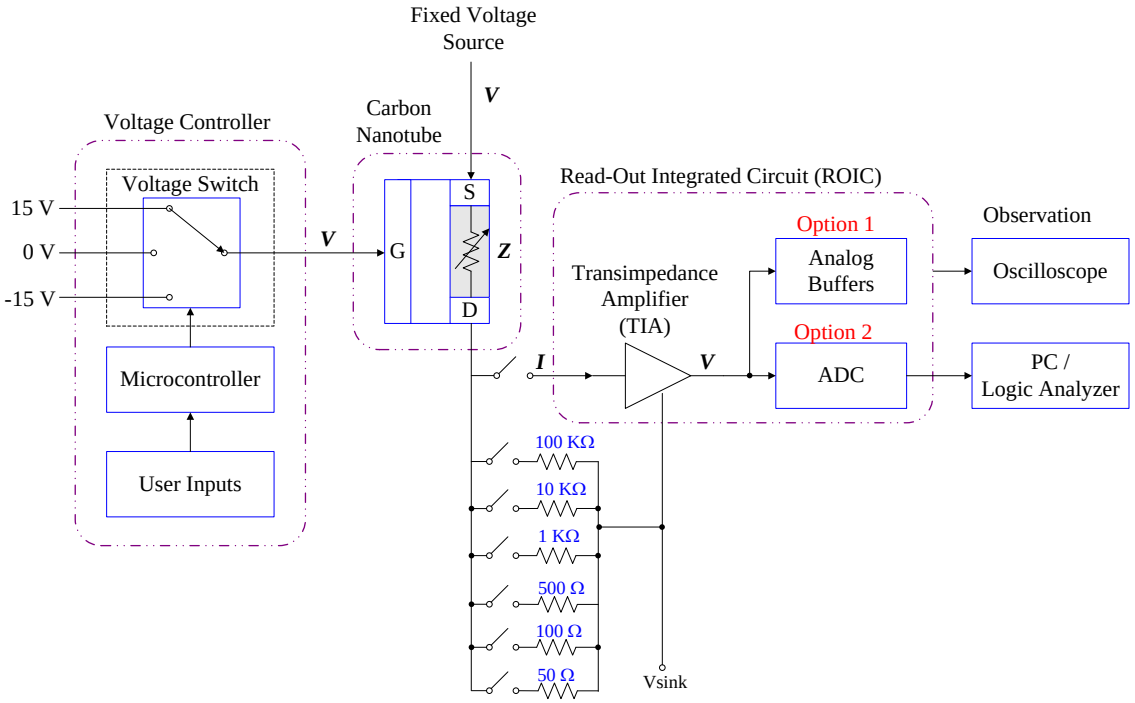

Figure 56 Expanded ROIC Usage.

Table 37 Expanded Sensor Current Detection Range.

I-to-V Conversion Mode	Tested Sensor Resistive Ranges	Current Detection Range
Primary TIA	9 MΩ - 25 MΩ (CNT)	8.4 nA – 46 nA
Secondary TIA	9 MΩ - 25 MΩ (CNT)	8.4 nA – 46 nA
100 KΩ	900 KΩ - 2.5 MΩ	84 nA – 460 nA
10 KΩ	90 KΩ - 250 KΩ	0.8 µA – 4.6 µA
1 KΩ	9 KΩ - 25 KΩ	8.4 µA – 46 µA
500 Ω	1.8 KΩ - 12.5 KΩ	16.8 µA – 227 µA
100 Ω	0.9 KΩ - 2.5 KΩ	84 µA – 456 µA
50 Ω	180 Ω - 250 Ω	168 µA – 2.27 mA

This facilitates the testing of other sensors, such as the Zinc Oxide (ZnO) gas sensor with the same sensor analysis system. The implemented mode selection circuitry is shown in Figure 57.

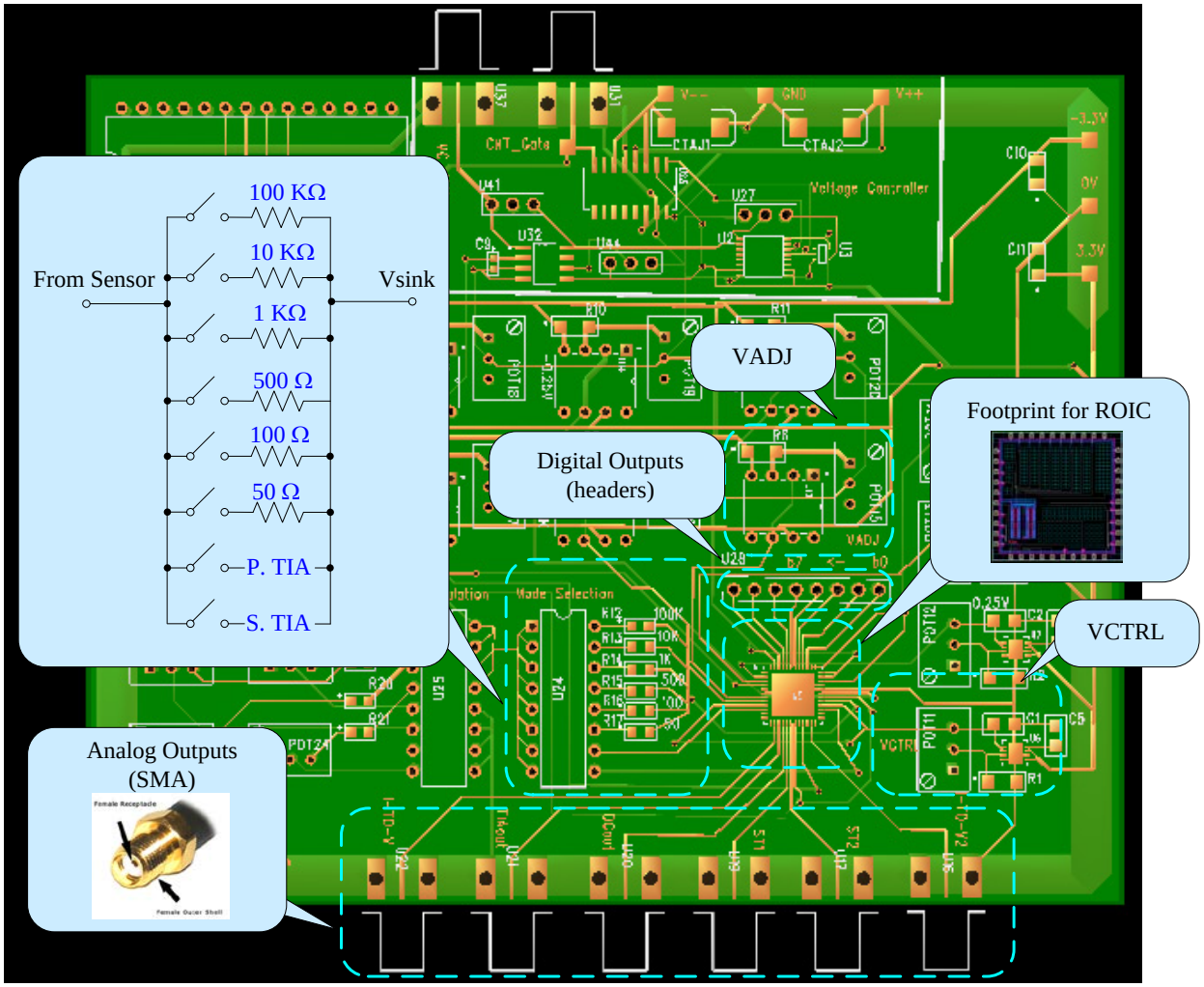

Figure 57 Mode Selection for Testing Other Sensor Profiles.

9.5.8 Phase I Prototype and Experimental Sensor Measurement Results

After communicating with Dr. Kim, he has prepared a ZnO sensor on the chip carrier and his measured results are shown in Figure 58 and Figure 59. These figures shows the excel plots of the source-to-drain current versus gate voltage based on the data he measured and recorded on the Excel sheets. He took his measurements in the AFRL facilities.

For our experimental setup, the sensor gate voltage is varied automatically from 5V, 0V, then to -5V on 2 second intervals through our voltage controller design. With AFRL's sensor source set at 0 volts and the drain connected to our current to voltage convertor, a snapshot of an actual output result is shown in Figure 60 when the measurement data is taken at Wright State University.

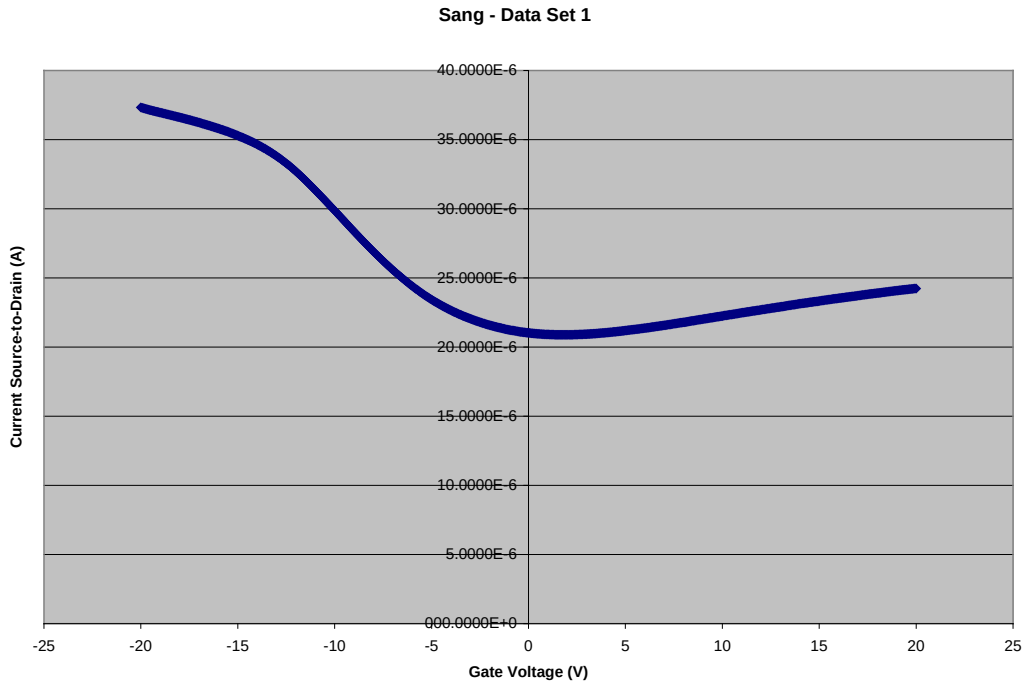

Figure 58 Reference Dataset From Sensor.

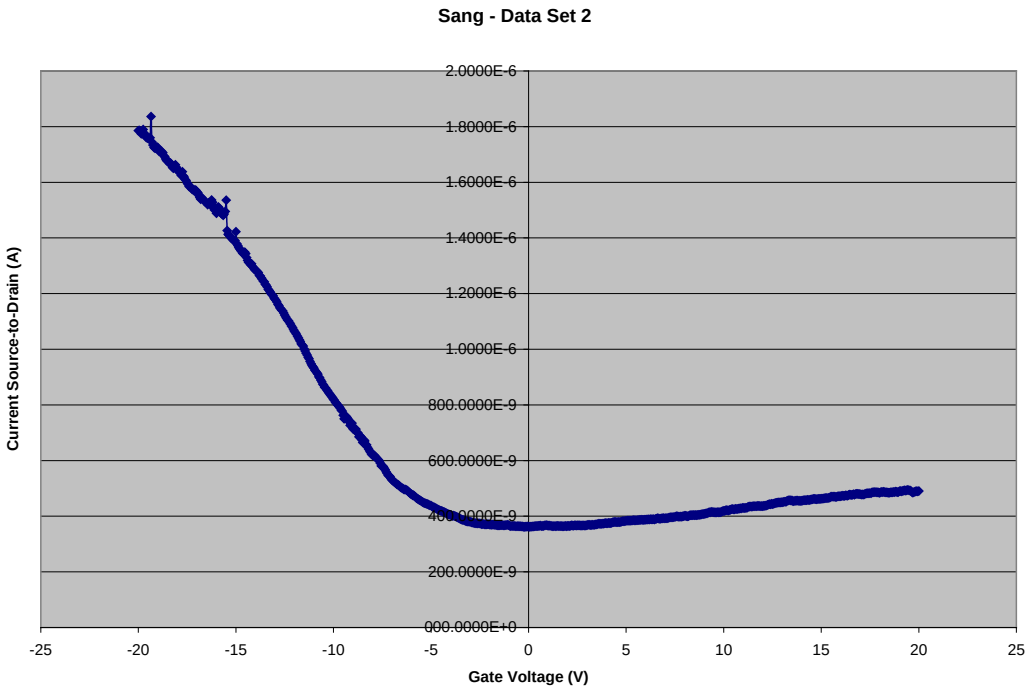

Figure 59 Reference Dataset from another Sensor.

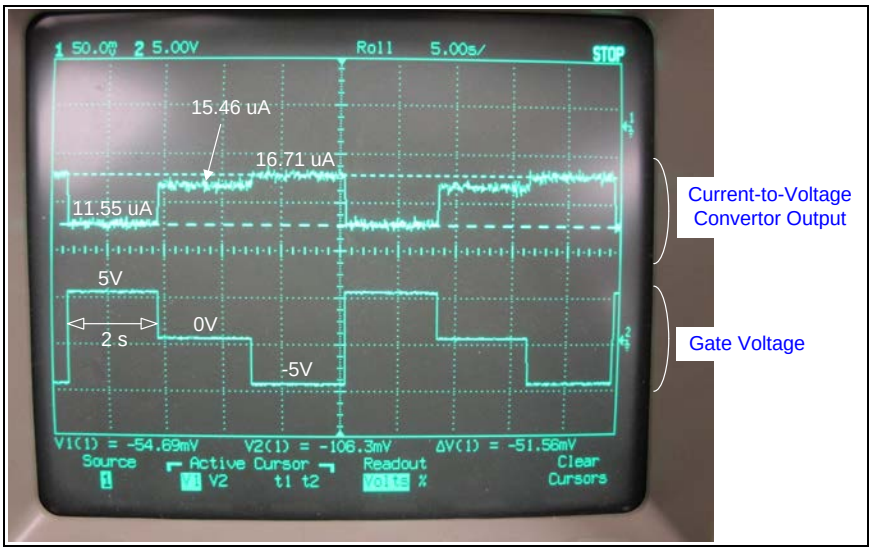

Figure 60 Oscilloscope Snapshot.

The top waveform in Figure 60 is the output from one of the high precision resistors populated on the chip for higher current measurements. When this high precision resistor is coupled in parallel with our chip to make use of the buffered chip outputs, the signal will be a bit noisier. Using the idea of voltage dividers noted in previous short reports, the current through the sensor can be computed easily from the output voltage. The source-to-drain current values for this snapshot are noted in Figure 60.

The experiment is repeated for gate voltages of ±10V to ±3V. The accumulated source-to-drain current versus sensor gate voltage data is plotted in Figure 61. This plot is based on the output voltage results from the readout integrated circuit in our work.

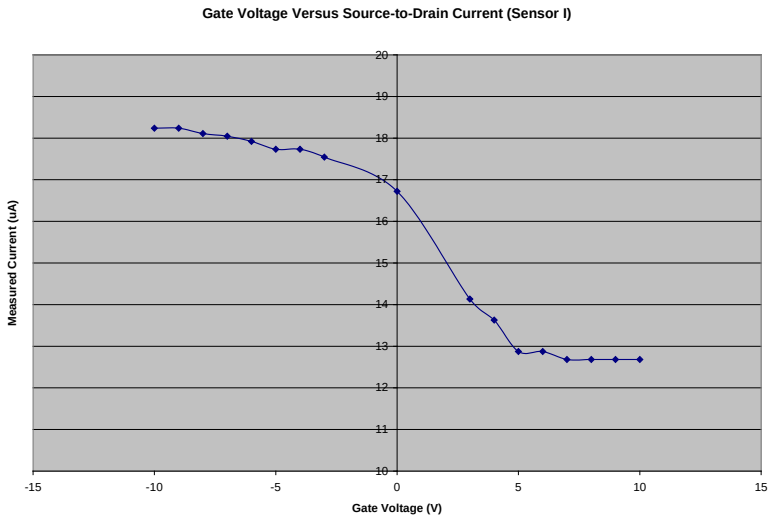

Figure 61 Measured Source-to-Drain Current Results from Readout Integrated Circuit Output.

The measured current results varied from 18.24 μA to 12.68 μA with an increase in sensor gate voltage. The trend of the current change is fairly similar to the measurement results taken at AFRL. However the environment impact at the lab in Wright State University is uncertain in comparison to AFRL's research labs. Dr. Kim's sensor measurement shows a current change from 37 μA to 21 μA in one sensor, and 1.8 μA to 0.36 μA in another.

Figure 62 and Figure 63 show the measured results when the gate voltage is varied every 3.9 ms and 16.4 ms. The computed current results are fairly similar with Figure 60.

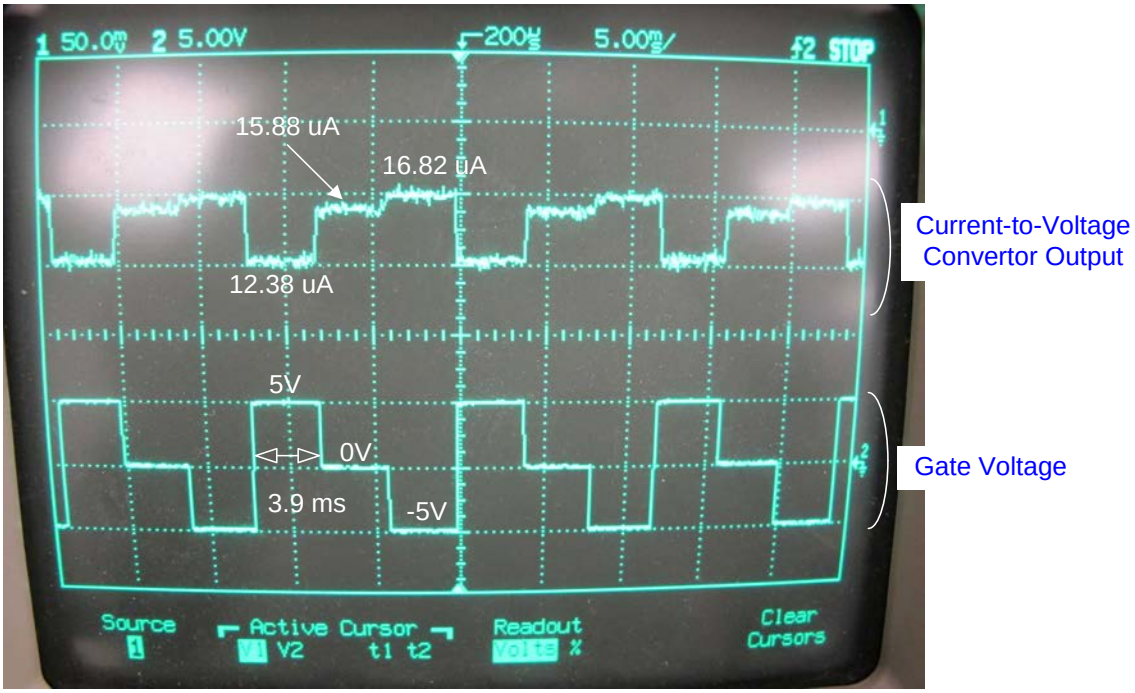

Figure 62 Oscilloscope Snapshot (t_{Δ}Vgate = 3.9 ms).

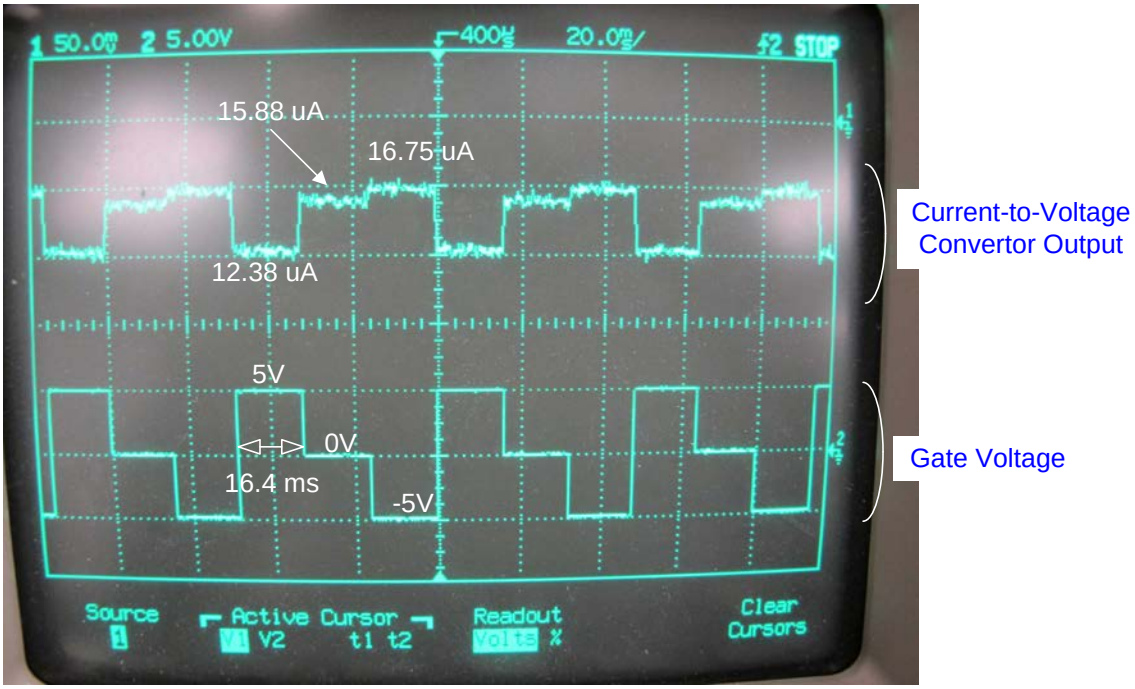

Figure 63 Oscilloscope Snapshot (t_{Δ}Vgate = 16.4 ms).

Figure 64 shows the current measurement setup, with two voltage supplies, one signal generator, and one oscilloscope for taking measurements. The voltage supplies are used for easy of adjustment and measurement purposes, this may be reduced further in future board design requirements. Figure 65 is a snapshot of the current PCB board with the voltage controller near the top and the readout integrated circuit in the bottom right. Figure 66 shows the present sensor connection to the board.

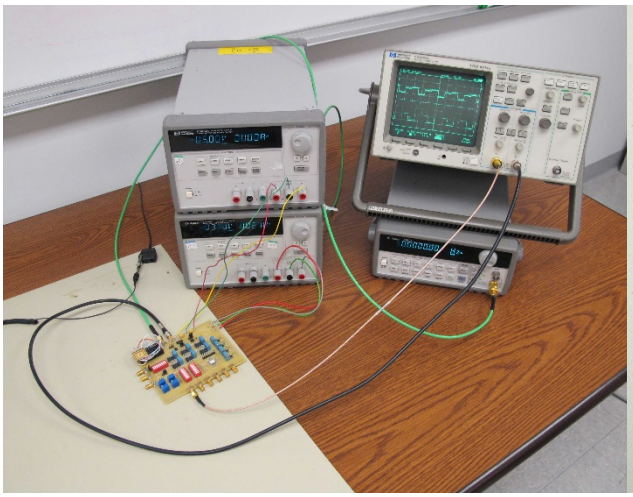

Figure 64 Testbed Setup.

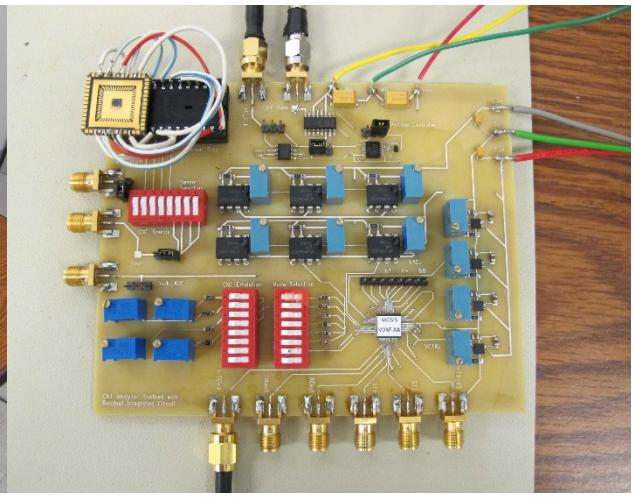

Figure 65 PCB Board Design.

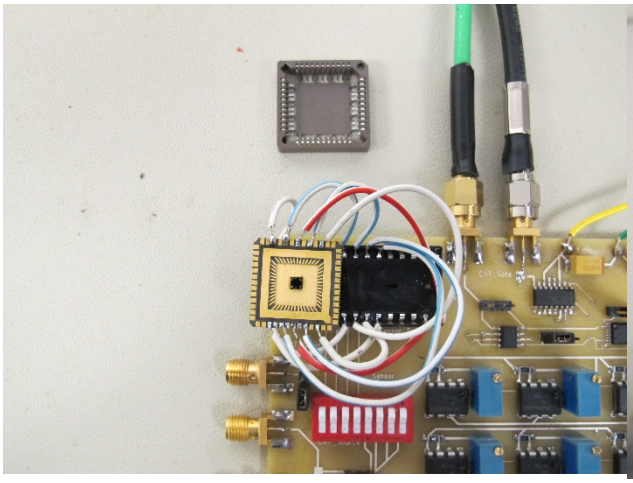

Figure 66 Sensor to Board Connection.

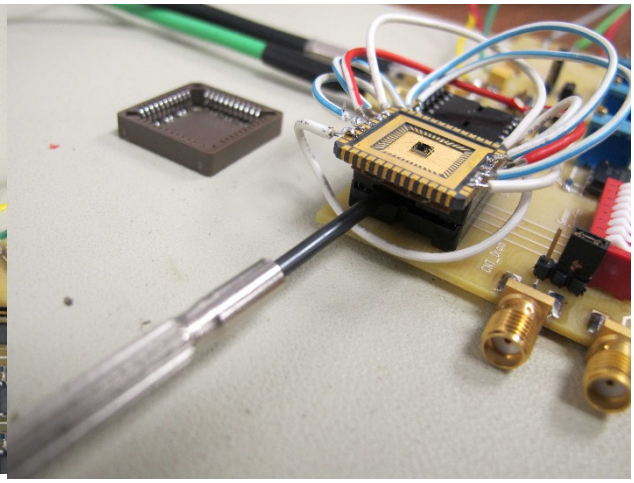

Figure 67 Easily Removable Sensor.

However, in future iterations of this board design, we may replace the 28-pin cover dip package with a socket similar to the grey one shown in Figure 66. We worked with Dr. Kim in trying a couple ways to bond the sensor to the dip packages, but Dr. Kim later find this gold open cavity chip package to work best with the equipment he had available. At that time, we already had the

board made and soldered with the components needed. It was too late to make another board for it. Figure 67 is a side shot to show that the sensor is easily detachable and can be replaced with other sensors of interest.

9.5.9 Conclusion and Future Work

Technical interchanges with Dr. Sang Nyon Kim were helpful in acquiring the measurement data and defining the design specifications. The authors would like to acknowledge the amount of time and effort he presented from the beginning to the completion of this pilot program. The current prototype has significantly surpassed beyond the initial design requirements. The current sensor analysis system allows a wider current detection range for testing different types of sensors. The designed PCB board is also tested with a ZnO sensor and shows comparable measurement results.

Future work includes further miniaturization of the number components used in the PCB with more stringent design requirements for simultaneous measurement of multiple sensor nodes. The experience and knowledge acquired from the first phase of the project allows better system definition for future generation of sensing boards knowing the limitation of the technology available. Since the final intention is to allow the system to be deployable to the field, further research work is needed to wirelessly transmit the measurement data and communicate with a central database. The current research community has also presented research work packaging gas sensors in a chip carrier with miniature gas inlets for letting gas pass through the sensor. This allows the analysis system to function without subjecting all the components to the unknown gaseous environment.

10 IMAGE TRUTHING (prepared by R. Myers)

10.1 Overview

Image truthing is the hand tracking objects of interest (vehicles and pedestrians) in wide area motion imagery via computer workstations. By hand tracking the objects, the actual location or "truth" of moving objects from frame to frame as well as the status of environmental operating conditions is determined and recorded. The data generated is useful to the Air Force Research Laboratory (AFRL) as a baseline to evaluate the performance of computer algorithms designed to detect and track objects in motion imagery. The imagery "truthed" is from various Air Force data collections.

AFRL's Mike Minardi and then Christopher Curtis served as Wright State University's direct client for this program.

In this program, Wright State University provided hourly paid Image Truthers, facilities, equipment, and supervisory and project management effort, as well as grant administration. AFRL provided servers, truther tools, data, technical training, and instruction. Wright State University's image truthing efforts, billed under fund 668664, began in 2011 and continued through Jun 30, 2015.

10.2 Technical Activities

An average of 30 image truthers provided 51,252 hours of truthing effort during the period of performance as depicted in the bi-weekly pay periods shown in Figure 68.

Beginning with 14 truthers in 2011, a total of 82 individual truthers were hired for this effort, with 23 continuing at the end of the period. A maximum roster of 44 active truthers was reached in early 2013. Billable hours per 2 week pay period ranged from 100.5 to 1326.5, with a mean of 528.4 hours per bi-weekly period. Five hiring cycles were utilized to coordinate worker availability with AFRL's data availability and throughput needs. No truthers were terminated due to lack of work.

All truthers were provided initial training, as well as periodic training and counseling to improve worker productivity, working environment, and compliance with the specific security requirements of certain data sets.

Most of the 82 truthers hired were university students, with the position providing income during their academic studies as well as tangible exposure to AFRL research important on a national and global scale. Truthers were hired with both a STEM focus and diversity as evident in the 23 working at the end of the period, 14 (61%) being College of Engineering and Computer Science students, and others from diverse areas including marketing, psychology, chemistry, and economics.

Truther supervision and project management were provided by Robert Myers, an employee of Wright State University and the Wright State Research Institute, at an average of 20 hours/month.

10.3 Facility

Image truthers work in a lab located in the Joshi Research Center, connected via hardwired LAN to a secure server room in the Joshi Research Center. Beginning with 14 work stations in 2011, an additional 10 computers were added in February 2013 to provide additional work station access. Lab security is provided via PIN access code locked door, truther training, and photo ID badges.

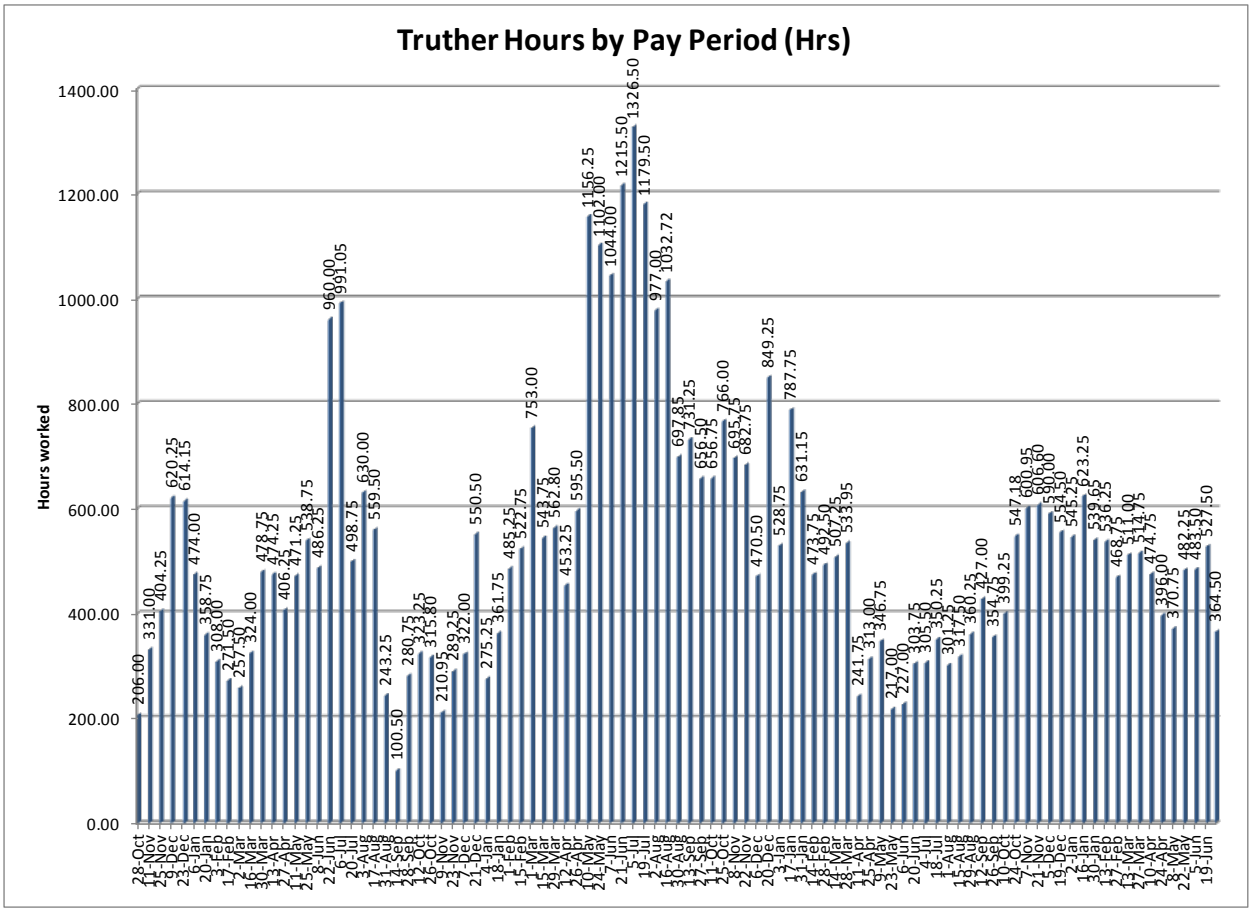

Figure 68 Image Truther effort by Pay Period (2011-2015).

11 RF TRANSMITTER LOCALIZATION VIA PHASE VARIANCE (prepared by Z. Wu)

11.1 Introduction

In this project, we have conducted research of a novel radio frequency (RF) transmitter localization algorithm using phase variance information.

Accurate passive source localization of unknown RF transmitters is an enabling capability within environmentally aware systems. If the localization of unknown RF transmitters can be obtained with sufficient accuracy, a variety of applications can be significantly enhanced. Such applications include cognitive radio (CR) and dynamic spectrum access (DSA) networks , software defined radar and passive radar. For passive radar systems that use emitters that are temporary or unknown, accurate knowledge of the transmitter location, together with some angular resolution is necessary in order to locate detected targets.

11.2 Phase Variance based RF Localization Algorithm

The algorithm described in this paper attempts to locate a single non-cooperative transmitter in a two dimensional plane using three or more directional receive antennas. The transmitted signal is assumed to be an isotropically propagating sine wave from a point source on a 2-D plane. It is important to note that our algorithm does not use the amplitude information at the receiver, hence the proposed algorithm works for both omnidirectional antenna and directional antenna at the non-cooperative RF transmitter being localized. We assume the signal source is coherently observed by three or more receivers which sample the signal at more than the required Nyquist rate. We also assume the signal include a multi-path component at amplitudes 0 and -40 dB relative to the direct path. The starting phase of the direct path signal is not known and estimation of this value is performed at the receivers. Additive white Gaussian noise of varying amplitudes is also added. We assume that the location of each receiver is known along with the antenna pattern of the receive antenna and the pointing angles of the receive antennae.

11.2.1 Known Phase at Transmitter

If we know the phase from the non-cooperative transmitter then the network of receivers localizes the transmitter as follows. In each case the composite signal at the receiver (SRX) consists of the signal that takes the direct path from the transmitter to the receiver (SDP), the multi-path signal from the transmitter to the receiver via the target or targets SMP , other signals SC, and noise _0.

The observed phase at the receiver is a combination of two phases: one is the phase at the transmitter at time zero, the second is a function of the range between the transmitter and the receiver. Triangulation using three directional antennas will result in a set of overlapping ellipses on a 2-D plane where the main lobes of the antennas intersect as shown in Figure 69. The

resulting enclosed area shown in red in the figure should contain the transmitter location. We assume this general geometry with three or more networked receivers.

Using the knowledge of the initial phase of the transmitter and the observed phase at each receiver it is possible to draw the wave fronts of equal phase across the enclosed area as shown in Figure 70. We can then select the potential locations of the transmitter where these lines intersect. These coordinates form the set of ambiguous potential transmitter locations.

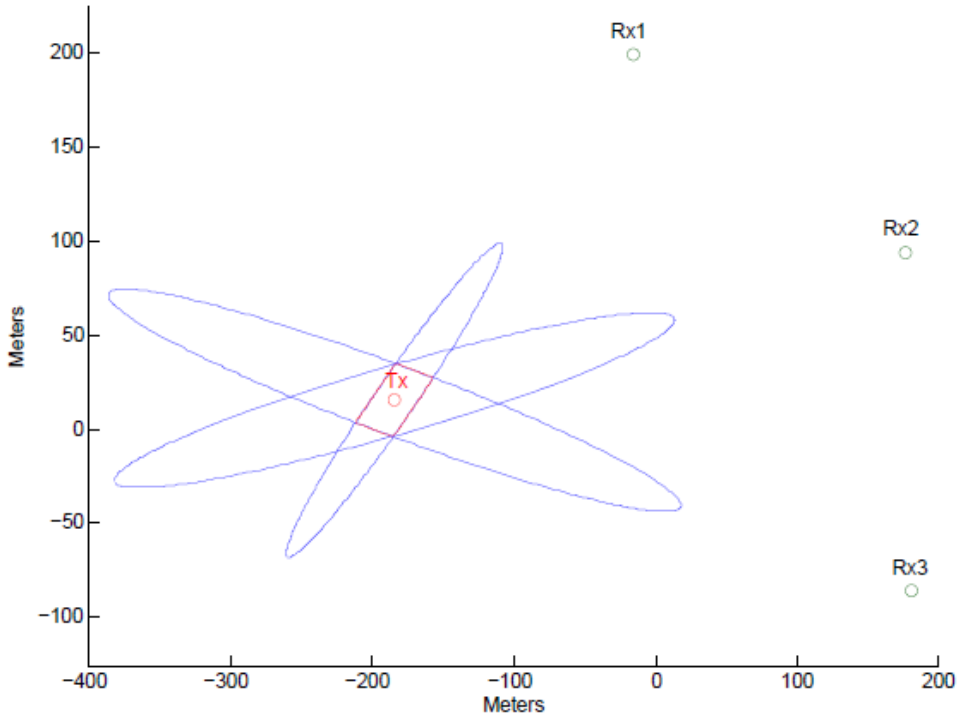

Figure 69 Overlapping Receiver Antenna Patterns.

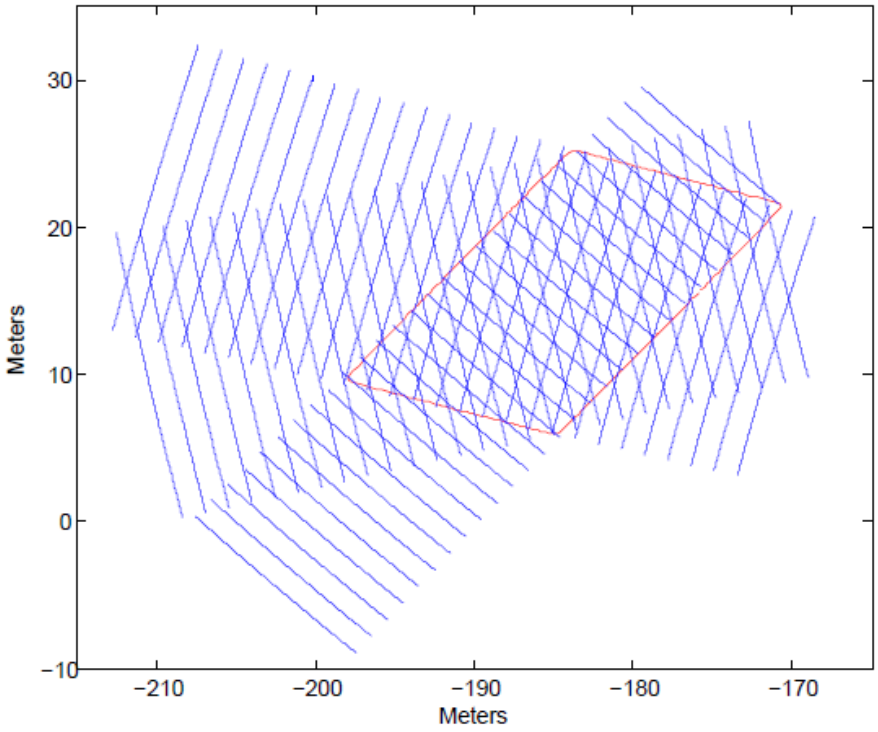

Figure 70 Enclosed Area.

11.2.2 Unknown Phase at Transmitter

In section 11.2.1, we assumed knowledge of the phase of the transmitter at time zero, a clearly unrealistic condition for non-cooperative transmitters. In this section we relax this condition and make estimation of the phase at each transmitter through the received phase at receiver antennas.

The received phase now has two components: the fractional wavelength resulting from the phase at the transmitter at time zero, and a function of range between the transmitter and the receiver. Because the transmitter is non-cooperative, the fraction of a wavelength resulting from phase at the origin will also need to be estimated. We assume that the receiver antennae beam patterns and where they are pointing are known. This knowledge allows us to find the ellipses where the antenna beam patterns intersect the 2-D plane. Traditional triangulation would find the signal peak of the overlapping antenna patterns and stop at this point.

If the antenna patterns overlap, searching p for local maxima leads to one or more potential transmitter locations. Because the total number of potential transmitter locations is small, an exhaustive search algorithm is feasible to find the best transmitter location and associated initial phase of the transmitter.

11.2.3 Numerical Results

Figure 71 shows an example of the numerical simulation of RF transmitter localization where 4 receivers are used. As shown in Figure 71, the proposed algorithm offers decent performance with low mean square error in the localization results.

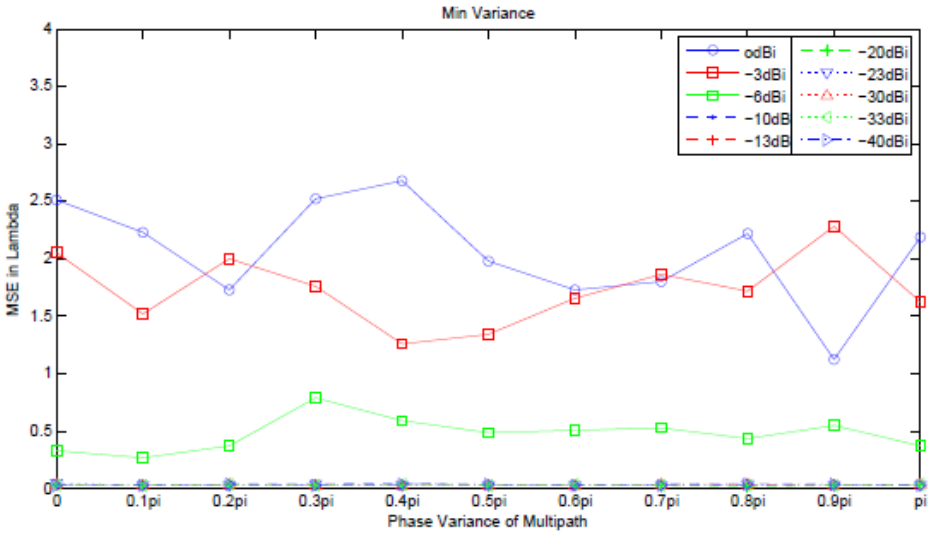

Figure 71 Simulation Result: MSE in Wavelength.

11.3 Conclusion

In this project, we have developed a RF localization algorithm based on phase variance information at receivers. It is shown that this algorithm provides accurate estimation of the RF locations. When coupled with other RF localization algorithms, more accurate localization is feasible.

11.4 Publication

[11] Charles Berdanier, Michael Wicks and Zhiqiang Wu, “Phase Based 2-D Passive Source Localization Using Receiver Networks,” accepted by *IET Radar, Sonar & Navigation*

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13 LIST OF SYMBOLS, ABBREVIATIONS, ACRONYMS

ACRONYM	DESCRIPTION
ADC	Analog Digital Converter
ATR	Automatic Target Recognition
ATRC	ATR Center
CMA-HT	Crowd Motion Analysis based on Heat Transfer
CMOS	Complementary Metal–Oxide–Semiconductor
CNN	Convolution Neural Network
CNT	Carbon Nano Tube
CoSAR	Communication and Synthetic Aperture Radar
COTS	Commercial Of The Shelf
CR	Cognitive Radio
CRLB	Cramer-Rao lower bound
CSR	Center for Surveillance Research
DL	Deep Learning
DSA	Digital Spectrum Access
ENOB	Effective Number Of Bits
FAME	Fragment Association Matching Enhancement
FAT	Feature Aided Tracker
KECoM	Knowledge Enhanced Compressive Measurement
LADAR	Light Detection And Ranging
LTE	long term evolution
MCRLB	Modified Cramer-Rao lower bound
MIMO	Multiple Input and Multiple Output
OaA	Overlap and Add
ROIC	Read-Out Integrated Circuit
RTO	NATO
SAR	Synthetic Aperture Radar
SATE	Summer At The Edge
SDP	Signal, Direct Path
SDR	Software Defined Radio
SFDR	Spurious Free Dynamic Range
SINAD	Signal to Noise and Distortion Ratio
SRX	Signal at the Receiver
STAP	radar Space Time Adaptive Processing
TIA	Trans-Impedance Amplifier
UMTS	universal mobile telecommunications signals
USRP	Universal Software Defined Radio Peripheral
VDL	Virtual Distributed Laboratory
ViDL	Virtual Discovery Lab
YATE	Year At The Edge